


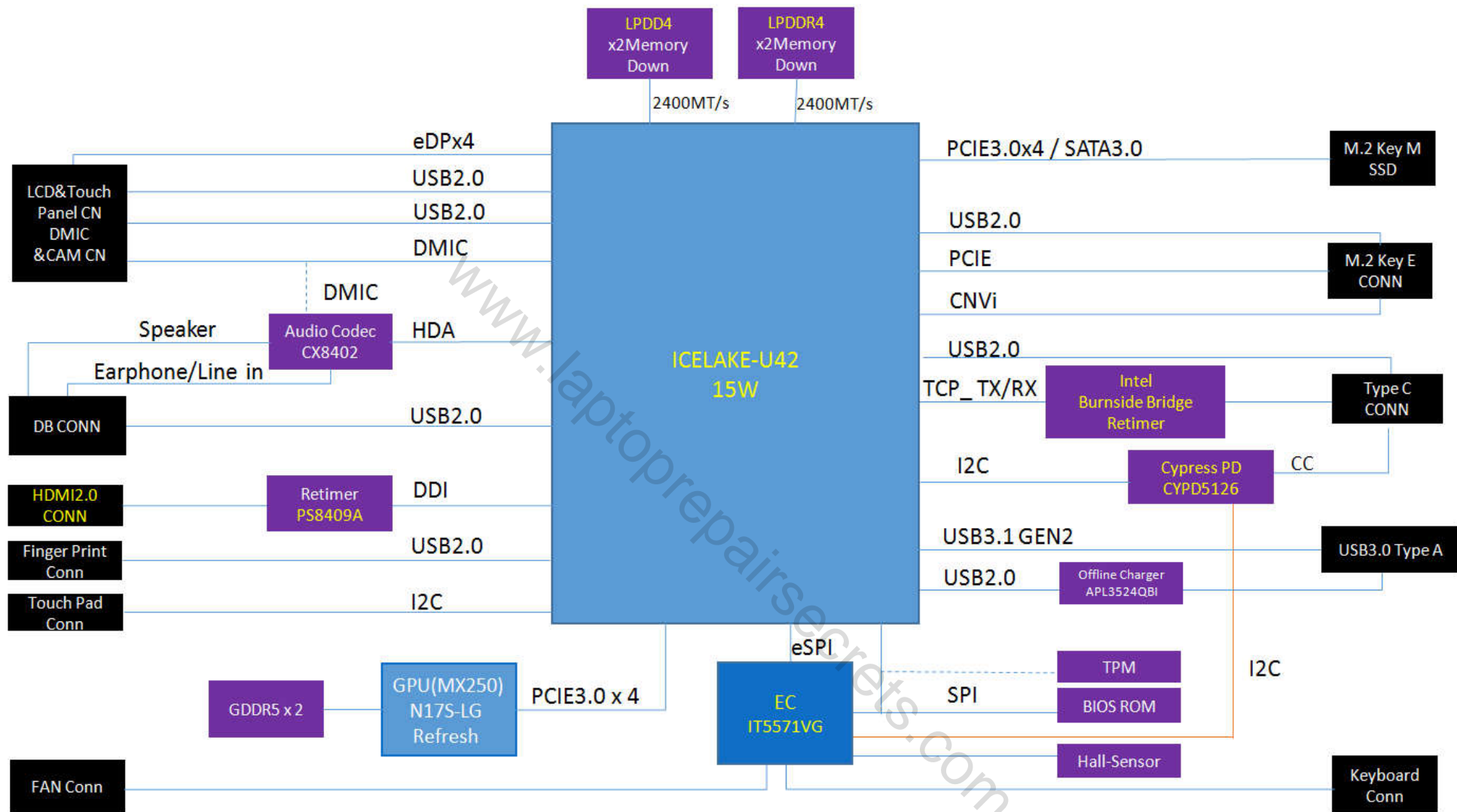
# HuaQin Confidential

## NB8511/12\_M/B Schematics Document Intel ICL Lake U-Processor with LPDDR4

REV1.0

2019-02-01

|          |                         |   |                             |           |
|----------|-------------------------|---|-----------------------------|-----------|
| Author   | Leo.Liu & Payne.Zhang   |  Huaqin Telecom Technology Com.,Ltd. |                             |           |
| Reviewer | Nelosn.Hai & Nemo.Jiang | Page name: <b>Cover page</b>  |                             |           |
| Approver | Lobo_Fan                | Size: A4  | Project Name: <b>NB8511</b> | REV: V1.0 |
|          |                         | Date: Monday, July 15, 2019   | Sheet: 1                    | of 72     |



**MEM ID**

| HW_ID3 | HW_ID2 | HW_ID1 | HW_ID0 | Description  | Total |
|--------|--------|--------|--------|--|-------|
| 0      | 0      | 0      | 0      | SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20          | 4GB   |
| 0      | 0      | 0      | 1      | HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP         | 4GB   |
| 0      | 0      | 1      | 0      | MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N | 8GB   |
| 0      | 1      | 0      | 0      | HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE          | 8GB   |
| 0      | 1      | 0      | 0      |  | 16GB  |
| 1      | 0      | 0      | 0      | HYNIX LPDDR4X 4266 4GB H9HCNNNCFMALHR-NEE LF+HF QDP        |       |
|        |        |        |        | 4x 16Gb(reserve)   |       |

**GPU ID**

| HW_ID5 | HW_ID4 | Description    |        |
|--------|--------|----------------|--------|
|        |        | N17-LG-Refresh | N17-LG |
| 0      | 0      | NC             | NC     |
| 1      | 0      | Mount          |        |
| 1      | 1      |                | Mount  |
|        |        |                |        |
|        |        |                |        |

**KB BL ID**


| HW_ID6 | Description           |
|--------|-----------------------|
| 0      | No keyboard Backlight |
| 1      | Keyboard Backlight    |

**Reserve ID**

| HW_ID7 | Description |
|--------|-------------|
| 0      | Reserve     |
| 1      | Reserve     |

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| Size:<br>A4   | Project<br>Name: <b>NB8511</b> | REV:<br>V1.0                        |  |
| Date:<br>Monday, July 15, 2019  | Sheet: <b>4</b>                | of <b>72</b>                        |  |



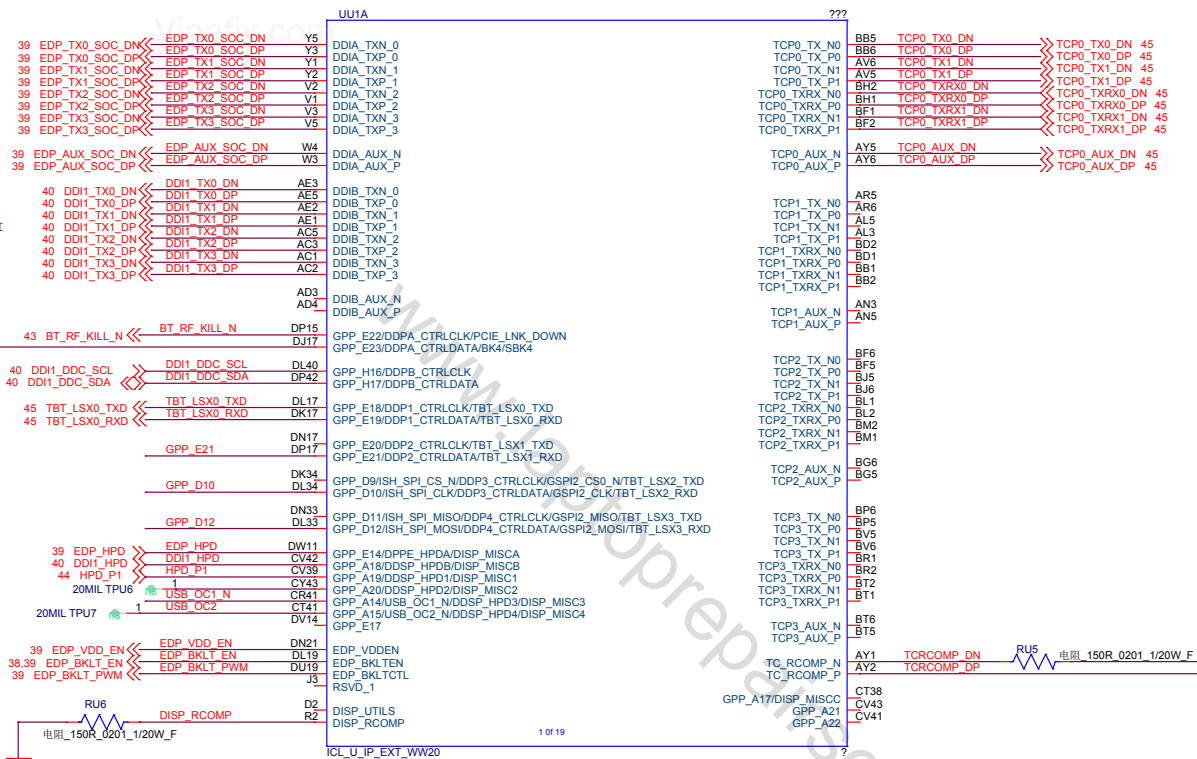
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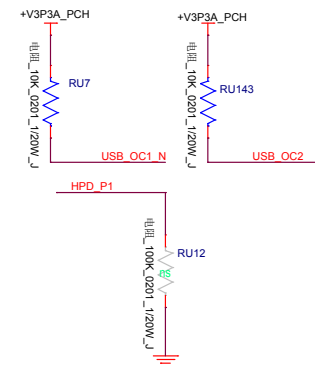
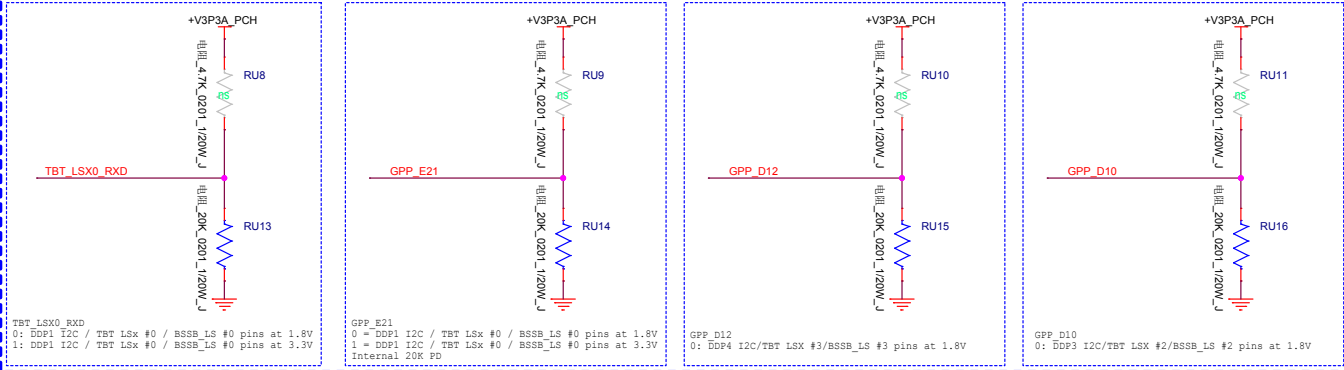
3 of 19

+V3P3A\_PCH

HDMI

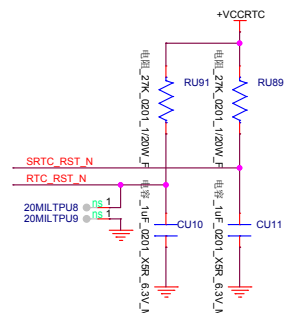
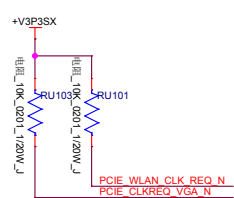


## PCH STRAP---VCCIO CONFIGURATION











GPU

29 PCIE\_CRX\_GTX\_N2 >>> PCIE CRX GTX N2  
29 PCIE\_CRX\_GTX\_P2 >>> PCIE CRX GTX P2  
29 PCIE\_CTX\_GRX\_N2 >>> PCIE CTX GRX N2 C  
29 PCIE\_CTX\_GRX\_P2 >>> PCIE CTX GRX P2 C

NA

WLAN

43 PCIE\_WLAN\_RX\_DN >>> PCIE WLAN RX DN  
43 PCIE\_WLAN\_RX\_DP >>> PCIE WLAN RX DP  
43 PCIE\_WLAN\_TX\_DN >>> PCIE WLAN TX DN  
43 PCIE\_WLAN\_TX\_DP >>> PCIE WLAN TX DP

SSD1

41 PCIE13\_CRX\_DTX\_N >>> PCIE13\_CRX\_DTX\_N  
41 PCIE13\_CRX\_DTX\_P >>> PCIE13\_CRX\_DTX\_P  
41 PCIE13\_CTX\_DRX\_N >>> PCIE13\_CTX\_DRX\_N  
41 PCIE13\_CTX\_DRX\_P >>> PCIE13\_CTX\_DRX\_P

41 PCIE14\_CRX\_DTX\_N >>> PCIE14\_CRX\_DTX\_N  
41 PCIE14\_CRX\_DTX\_P >>> PCIE14\_CRX\_DTX\_P  
41 PCIE14\_CTX\_DRX\_N >>> PCIE14\_CTX\_DRX\_N  
41 PCIE14\_CTX\_DRX\_P >>> PCIE14\_CTX\_DRX\_P

41 PCIE15\_CRX\_DTX\_N >>> PCIE15\_CRX\_DTX\_N  
41 PCIE15\_CRX\_DTX\_P >>> PCIE15\_CRX\_DTX\_P  
41 PCIE15\_CTX\_DRX\_N >>> PCIE15\_CTX\_DRX\_N  
41 PCIE15\_CTX\_DRX\_P >>> PCIE15\_CTX\_DRX\_P

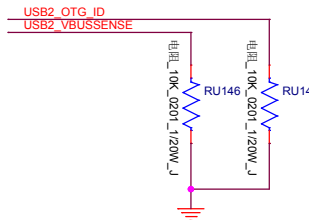
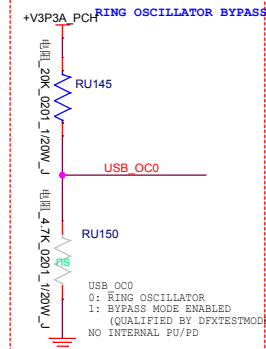
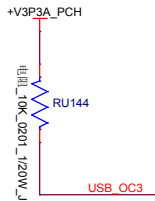
41 PCIE16\_SATA\_CRX\_DTX\_N >>> PCIE16\_SATA\_CRX\_DTX\_N  
41 PCIE16\_SATA\_CRX\_DTX\_P >>> PCIE16\_SATA\_CRX\_DTX\_P  
41 PCIE16\_SATA\_CTX\_DRX\_N >>> PCIE16\_SATA\_CTX\_DRX\_N  
41 PCIE16\_SATA\_CTX\_DRX\_P >>> PCIE16\_SATA\_CTX\_DRX\_P

10.41 SSD1\_DET >>> SSD1\_DET  
49 USB\_OC0 >>> USB\_OC0  
54 USB\_OC3 >>> USB\_OC3

41 SATA1\_DEVS\_LP <<< SATA1\_DEVS\_LP

RU142 电阻 100R\_0201\_1/20W\_F  
PCIE\_RCOMP\_N  
PCIE\_RCOMP\_P

## PCH STRAP



U01H

777

CV7 PCIE7\_RXN  
CV6 PCIE7\_RXP  
DD3 PCIE7\_TXN  
DD5 PCIE7\_TXP

CT6 PCIE8\_RXN  
CT7 PCIE8\_RXP  
DA3 PCIE8\_TXN  
DA5 PCIE8\_TXP

CP6 PCIE9\_RXN  
DA2 PCIE9\_RXP  
DA1 PCIE9\_TXN  
PCIE9\_TXP

CM7 PCIE10\_RXN  
CM6 PCIE10\_RXP  
CY3 PCIE10\_TXN  
CY4 PCIE10\_TXP

CK7 PCIE11\_RXN/SATA0\_RXN  
CK6 PCIE11\_RXP/SATA0\_RXP  
CW2 PCIE11\_TXN/SATA0\_TXN  
CW1 PCIE11\_TXP/SATA0\_TXP

CJ6 PCIE12\_RXN/SATA1A\_RXN  
CJ7 PCIE12\_RXP/SATA1A\_RXP  
CW5 PCIE12\_TXN/SATA1A\_TXN  
CW3 PCIE12\_TXP/SATA1A\_TXP

CG7 PCIE13\_RXN  
CG6 PCIE13\_RXP  
CT3 PCIE13\_TXN  
CT5 PCIE13\_TXP

CE6 PCIE14\_RXN  
CE7 PCIE14\_RXP  
CT2 PCIE14\_TXN  
CT1 PCIE14\_TXP

CC5 PCIE15\_RXN/SATA1B\_RXN  
CC6 PCIE15\_RXP/SATA1B\_RXP  
CR3 PCIE15\_TXN/SATA1B\_TXN  
CR4 PCIE15\_TXP/SATA1B\_TXP

CA6 PCIE16\_RXN/SATA2\_RXN  
CA5 PCIE16\_RXP/SATA2\_RXP  
CP1 PCIE16\_TXN/SATA2\_TXN  
CP2 PCIE16\_TXP/SATA2\_TXP

DW12 GPP\_E0/SATA0/PCIE0/SATAGP0  
CR43 GPP\_A12/SATA0/PCIE1/SATAGP1  
GPP\_A13/SATA0/PCIE2/SATAGP2

DW14 GPP\_E9/USB\_OC0\_N  
CT43 GPP\_A16/USB\_OC3\_N

DU11 GPP\_E4/DEVSLP0  
DU12 GPP\_E5/DEVSLP1  
CV48 GPP\_A11/DEVSLP2

DT38 GPP\_H12/M2\_SKT2\_CFG0  
DW38 GPP\_H13/M2\_SKT2\_CFG1  
DU38 GPP\_H14/M2\_SKT2\_CFG2  
GPP\_H15/M2\_SKT2\_CFG3

DN1 PCIE\_RCOMP\_N  
DN3 PCIE\_RCOMP\_P  
ICL\_U\_IP\_EXT\_WW20

PCIE1\_RXN/USB31\_1\_RXN  
PCIE1\_RXP/USB31\_1\_RXP  
PCIE1\_TXN/USB31\_1\_TXN  
PCIE1\_TXP/USB31\_1\_TXP

PCIE2\_RXN/USB31\_2\_RXN  
PCIE2\_RXP/USB31\_2\_RXP  
PCIE2\_TXN/USB31\_2\_TXN  
PCIE2\_TXP/USB31\_2\_TXP

PCIE3\_RXN/USB31\_3\_RXN  
PCIE3\_RXP/USB31\_3\_RXP  
PCIE3\_TXN/USB31\_3\_TXN  
PCIE3\_TXP/USB31\_3\_TXP

PCIE4\_RXN/USB31\_4\_RXN  
PCIE4\_RXP/USB31\_4\_RXP  
PCIE4\_TXN/USB31\_4\_TXN  
PCIE4\_TXP/USB31\_4\_TXP

PCIE5\_RXN/USB31\_5\_RXN  
PCIE5\_RXP/USB31\_5\_RXP  
PCIE5\_TXN/USB31\_5\_TXN  
PCIE5\_TXP/USB31\_5\_TXP

PCIE6\_RXN/USB31\_6\_RXN  
PCIE6\_RXP/USB31\_6\_RXP  
PCIE6\_TXN/USB31\_6\_TXN  
PCIE6\_TXP/USB31\_6\_TXP

USB2N\_1  
USB2P\_1

USB2N\_2  
USB2P\_2

USB2N\_3  
USB2P\_3

USB2N\_4  
USB2P\_4

USB2N\_5  
USB2P\_5

USB2N\_6  
USB2P\_6

USB2N\_7  
USB2P\_7

USB2N\_8  
USB2P\_8

USB2N\_9  
USB2P\_9

USB2N\_10  
USB2P\_10

USB\_ID

USB\_VBUSSENSE

USB2\_COMP

RSVD\_BSCAN

DJ8 USB3\_P1\_RX\_DN  
DJ6 USB3\_P1\_RX\_DP  
DJ2 USB3\_P1\_TX\_DN  
DJ1 USB3\_P1\_TX\_DP

DC9 PCIE2\_RXN/USB31\_2\_RXN  
DG7 PCIE2\_RXP/USB31\_2\_RXP  
DJ3 PCIE2\_TXN/USB31\_2\_TXN  
DJ5 PCIE2\_TXP/USB31\_2\_TXP

DE7 PCIE3\_RXN/USB31\_3\_RXN  
DE9 PCIE3\_RXP/USB31\_3\_RXP  
DF3 PCIE3\_TXN/USB31\_3\_TXN  
DF5 PCIE3\_TXP/USB31\_3\_TXP

DC7 PCIE4\_RXN/USB31\_4\_RXN  
DC9 PCIE4\_RXP/USB31\_4\_RXP  
DF2 PCIE4\_TXN/USB31\_4\_TXN  
DF1 PCIE4\_TXP/USB31\_4\_TXP

DA6 PCIE\_CRX\_GTX\_N0  
DA7 PCIE\_CRX\_GTX\_P0  
DE4 PCIE\_CTX\_GRX\_N0 C  
DE3 PCIE\_CTX\_GRX\_P0 C

CY7 PCIE\_CRX\_GTX\_N1  
CY6 PCIE\_CRX\_GTX\_P1  
DD1 PCIE\_CTX\_GRX\_N1 C  
DD2 PCIE\_CTX\_GRX\_P1 C

DN8 USB2\_P1\_DN  
DP8 USB2\_P1\_DP

DK11  
DJ11

DP13 USB2\_P3\_TYPEC\_DN  
DN13 USB2\_P3\_TYPEC\_DP

DK10 USB2\_P4\_DN  
DJ10 USB2\_P4\_DP

DL5 USB2\_P5\_FP\_DN  
DL3 USB2\_P5\_FP\_DP

DP11 USB\_P7\_CAM\_N  
DN11 USB\_P7\_CAM\_P

DK13  
DJ13

DN6  
DP6

DL2 USB2\_P9\_TS\_DN  
DL1 USB2\_P9\_TS\_DP

DP10 USB2\_P10\_BT\_DN  
DN10 USB2\_P10\_BT\_DP

DL6 USB2\_OTG\_ID

DL11 USB2\_VBUSSENSE

DN5 USB2\_COMP

CD3

USB3.0 TypeA 1 AUO

NA

NA

NA

USB3.0 Type-A 1 AUO

NA

Type-C

DB USB2.0 Type-A

Finger Print

Camera

NA

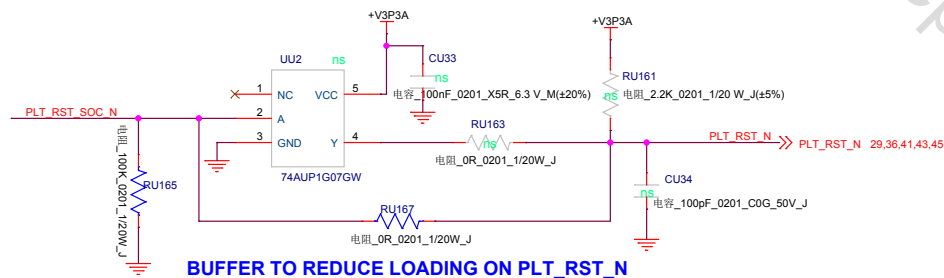
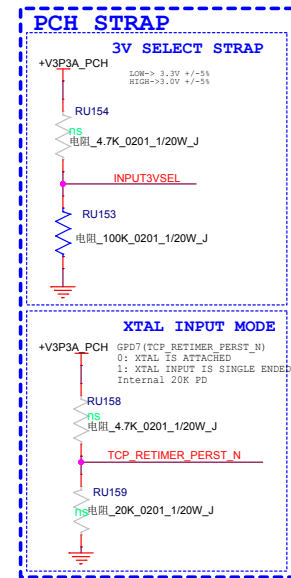
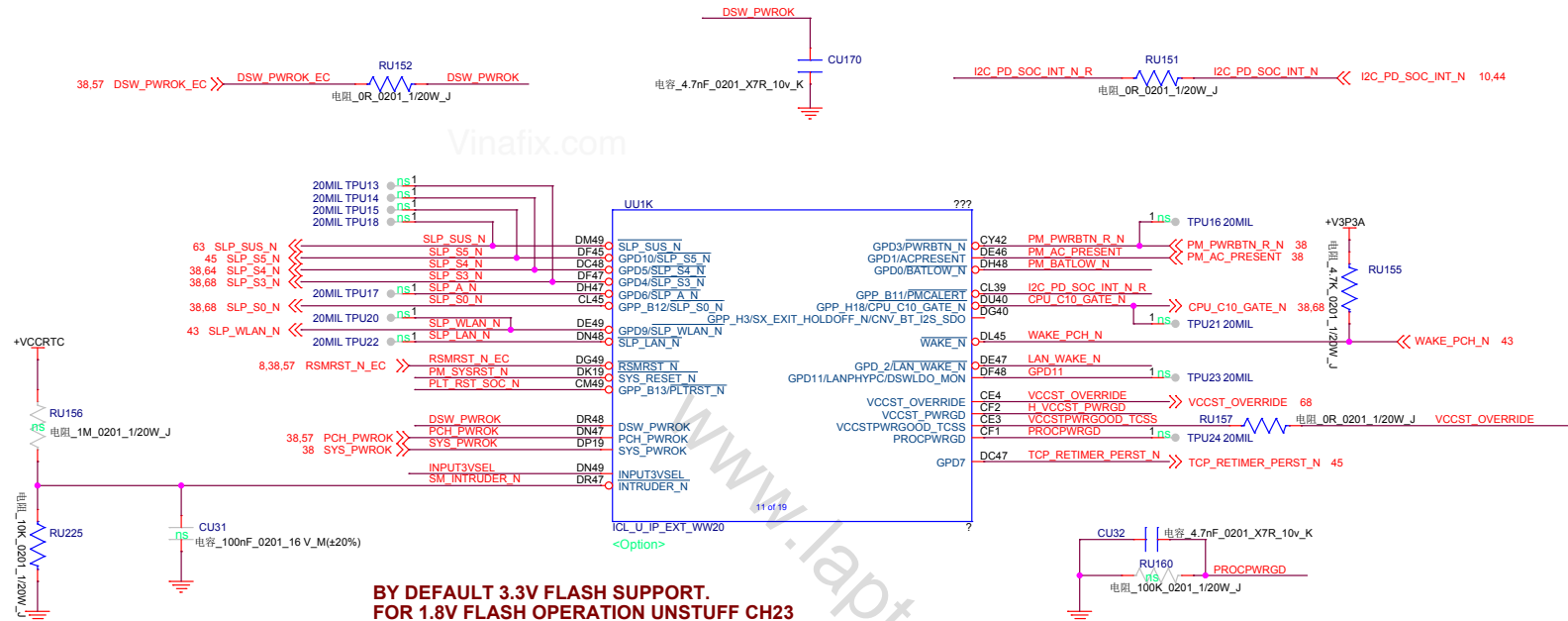
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Touch Panel

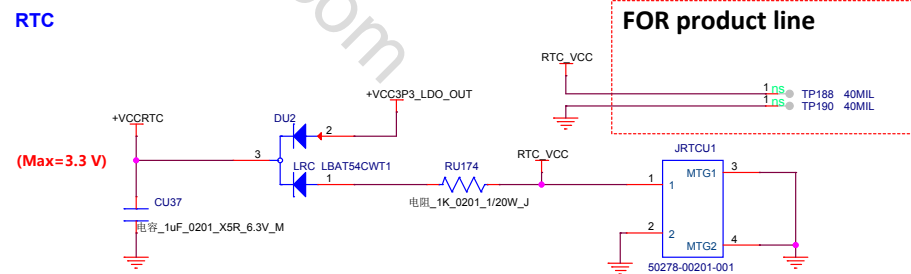
BT

GPU

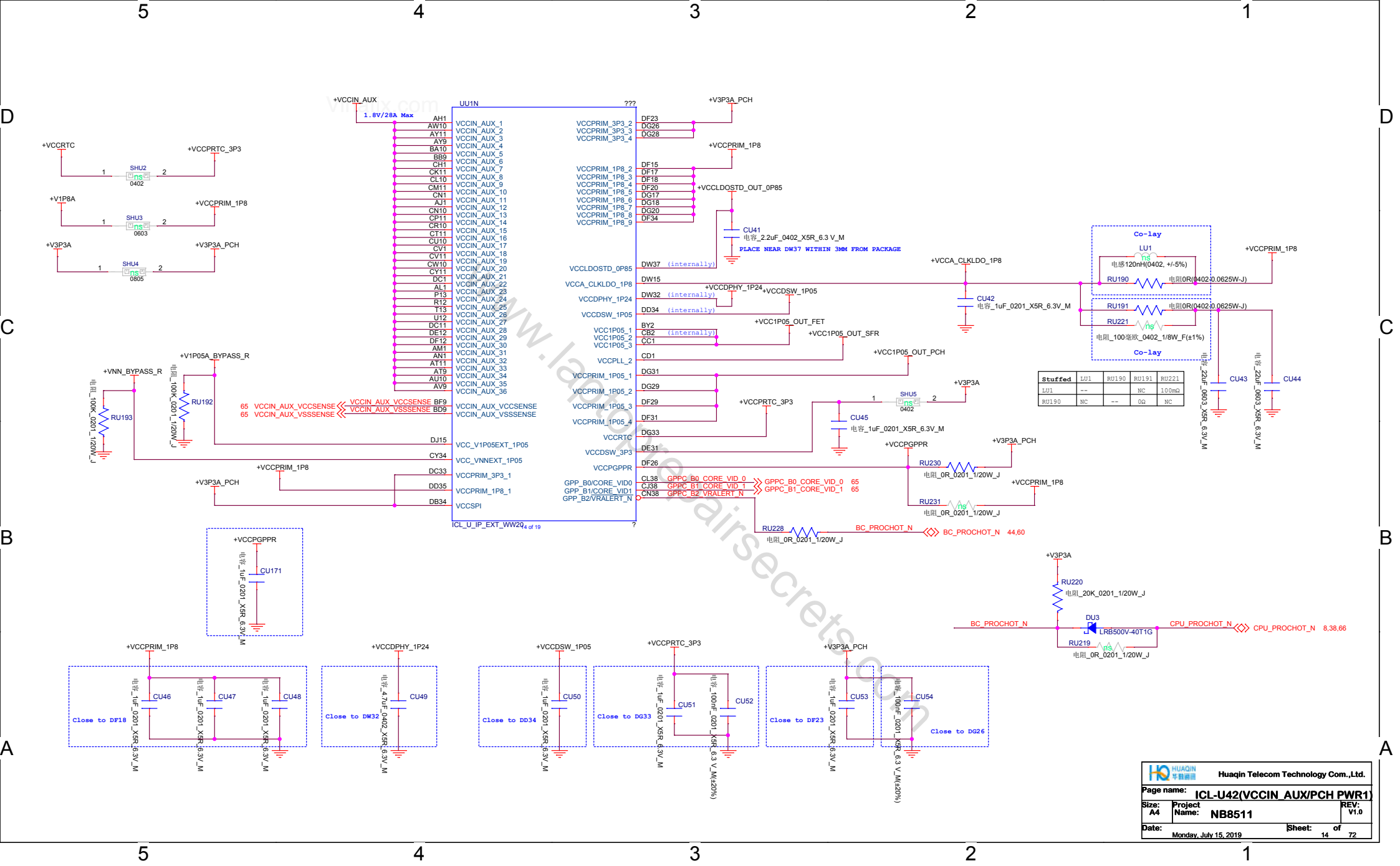
USB2\_COMP2 RESISTOR SHOULD  
BE PLACED NEAR TO THE PIN  
LENGHT <450 MILS



## RTC

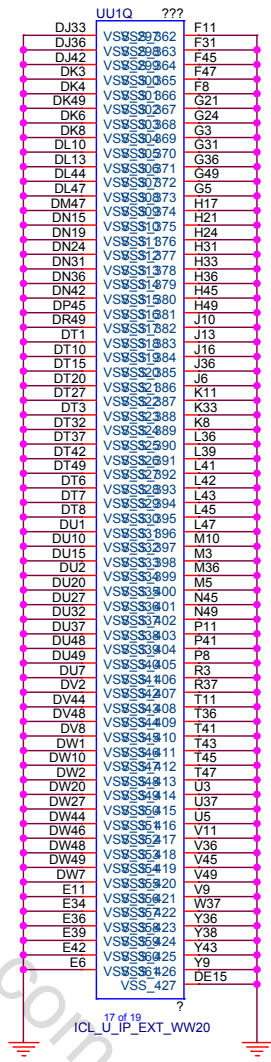
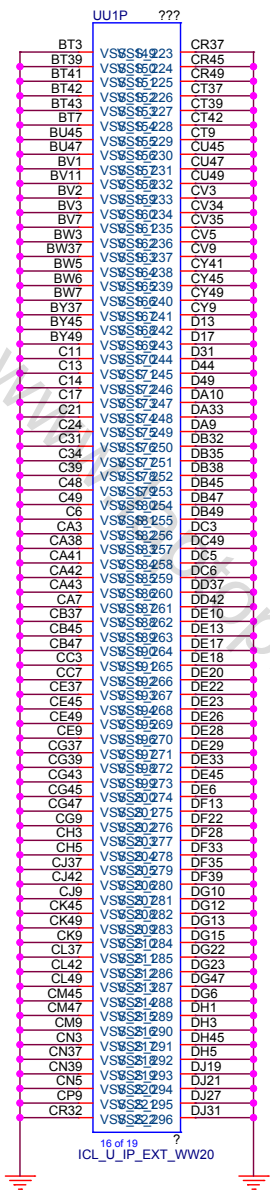
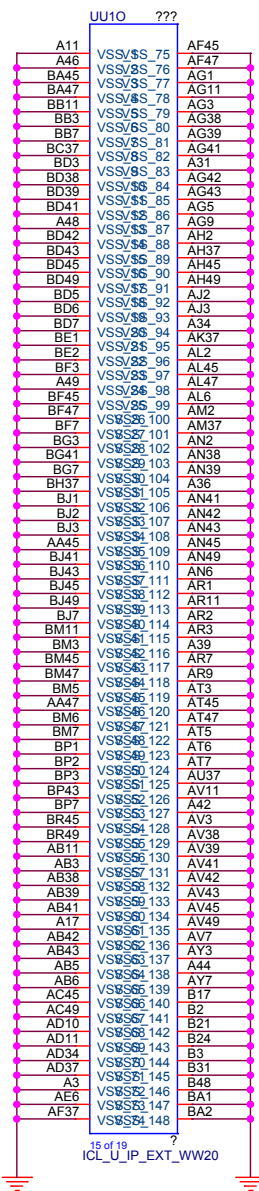




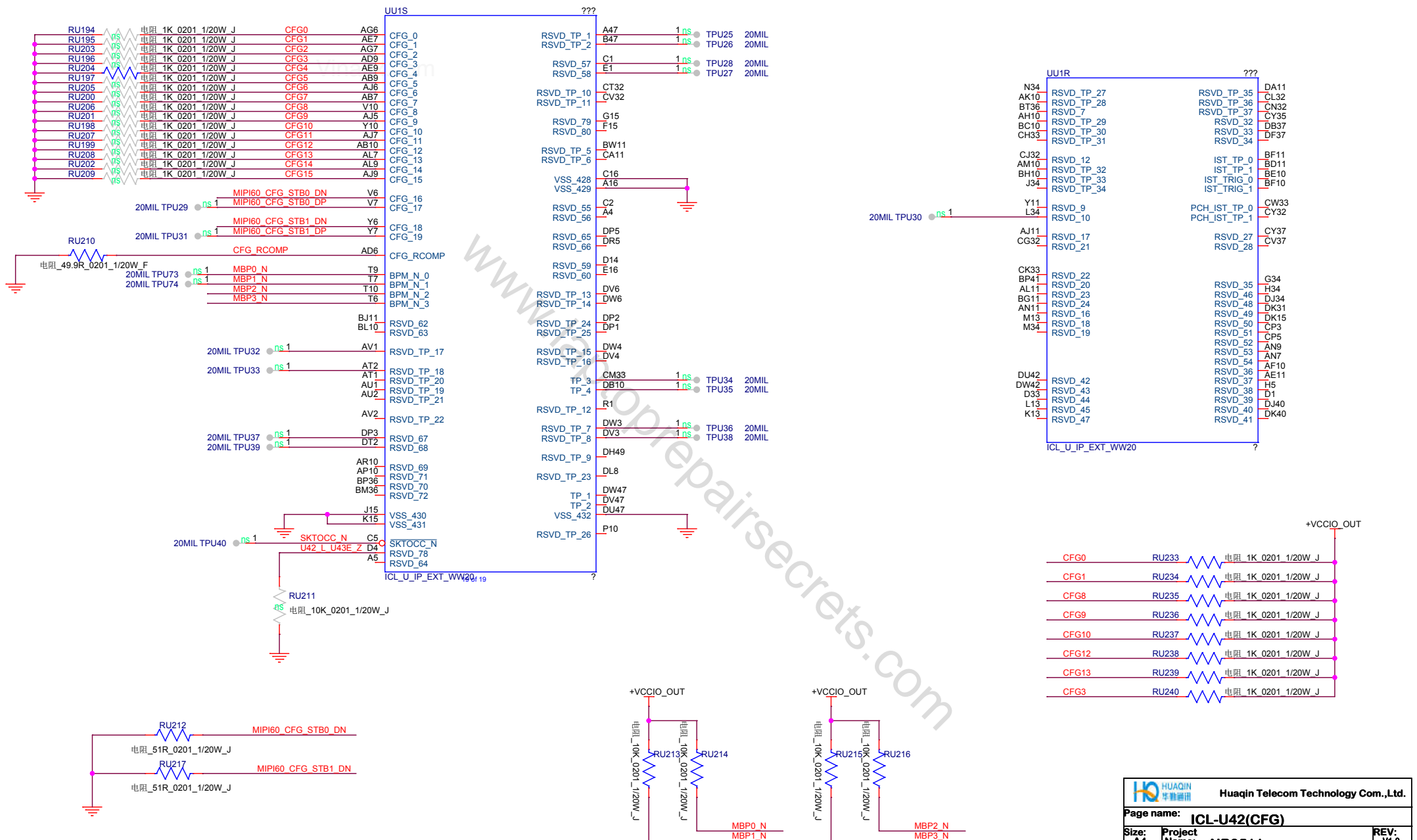


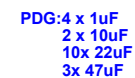


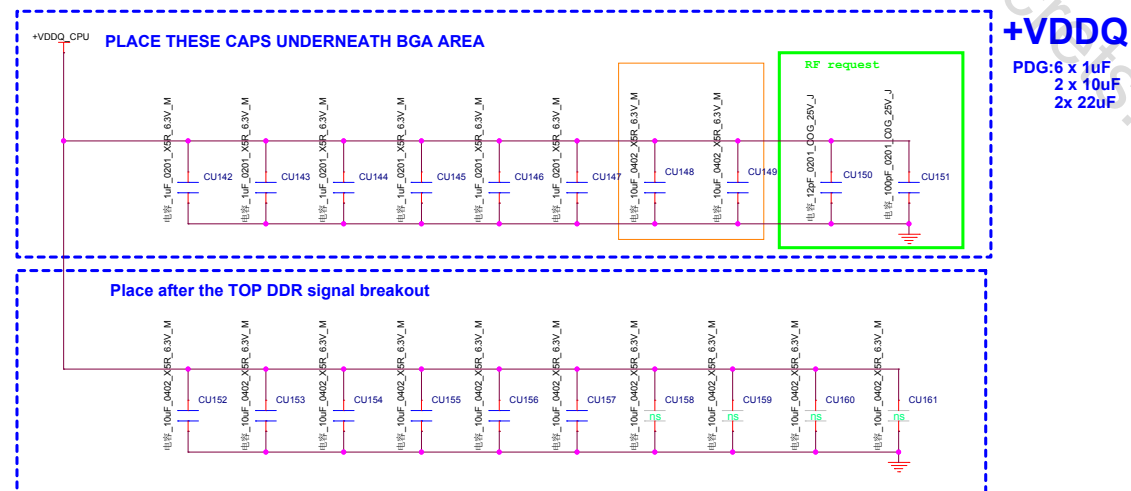
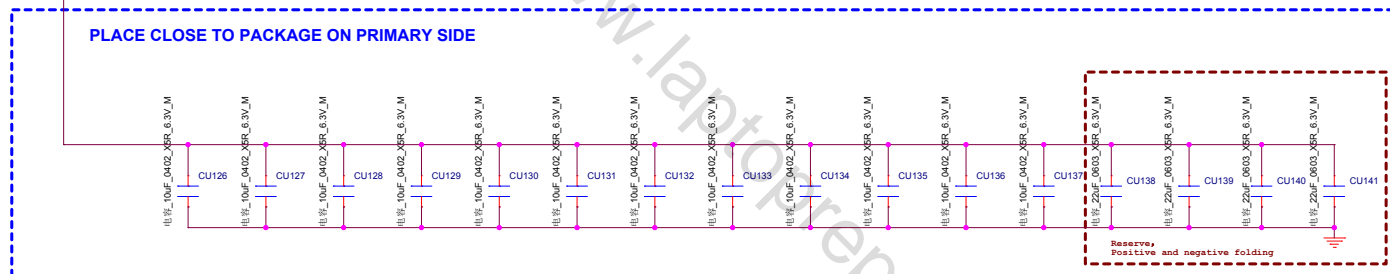
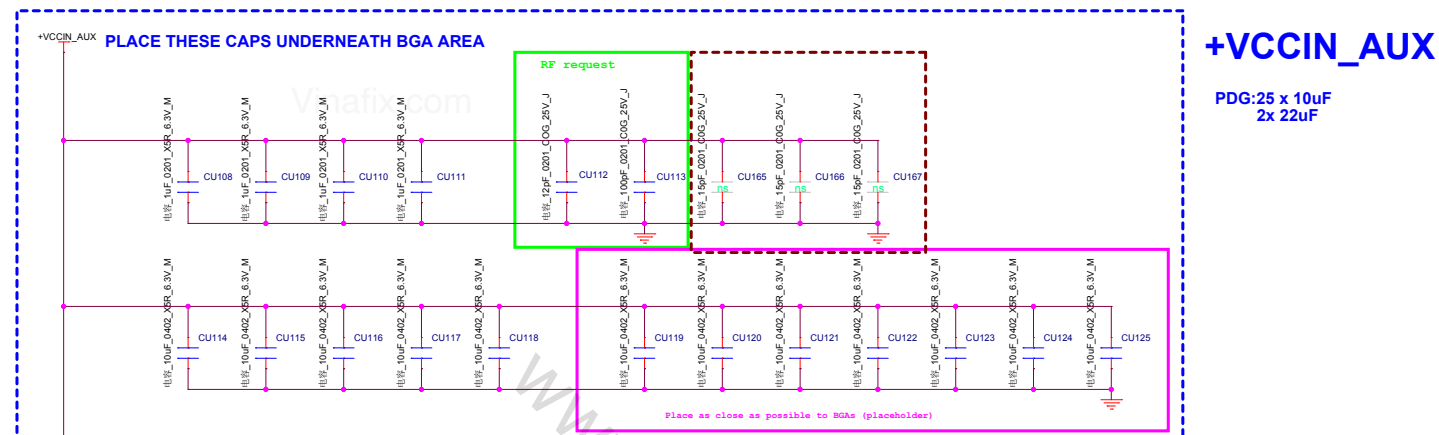









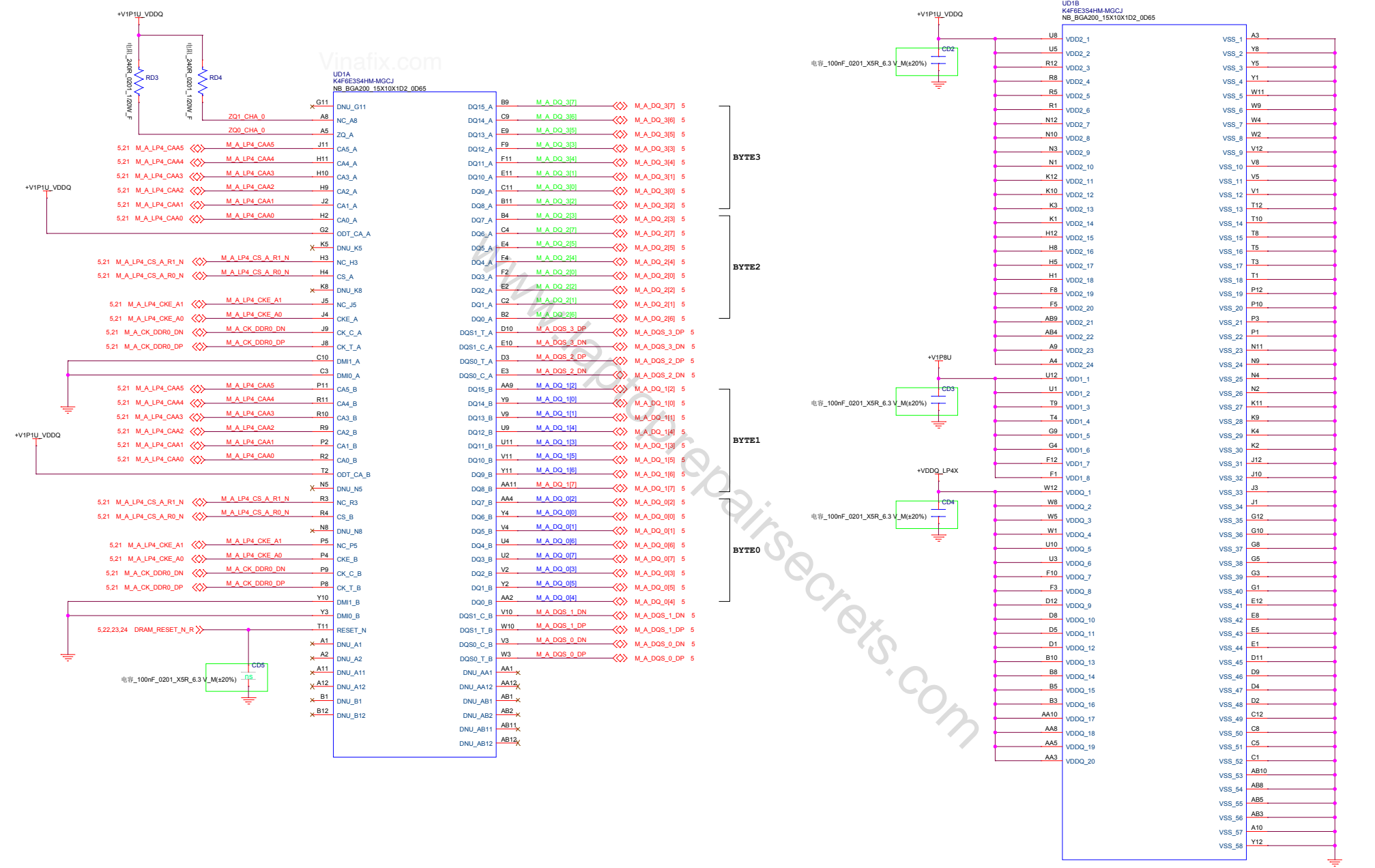


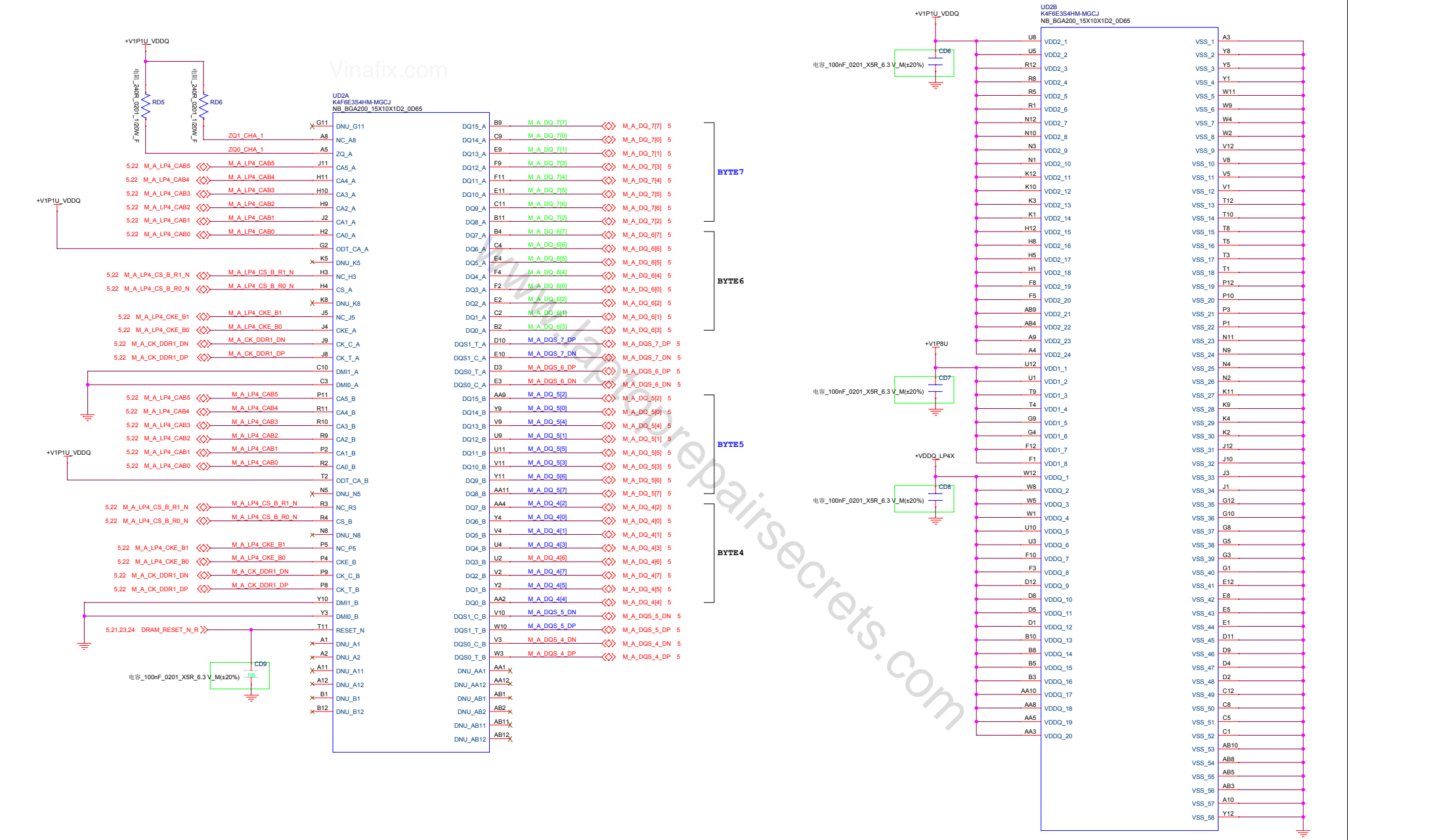


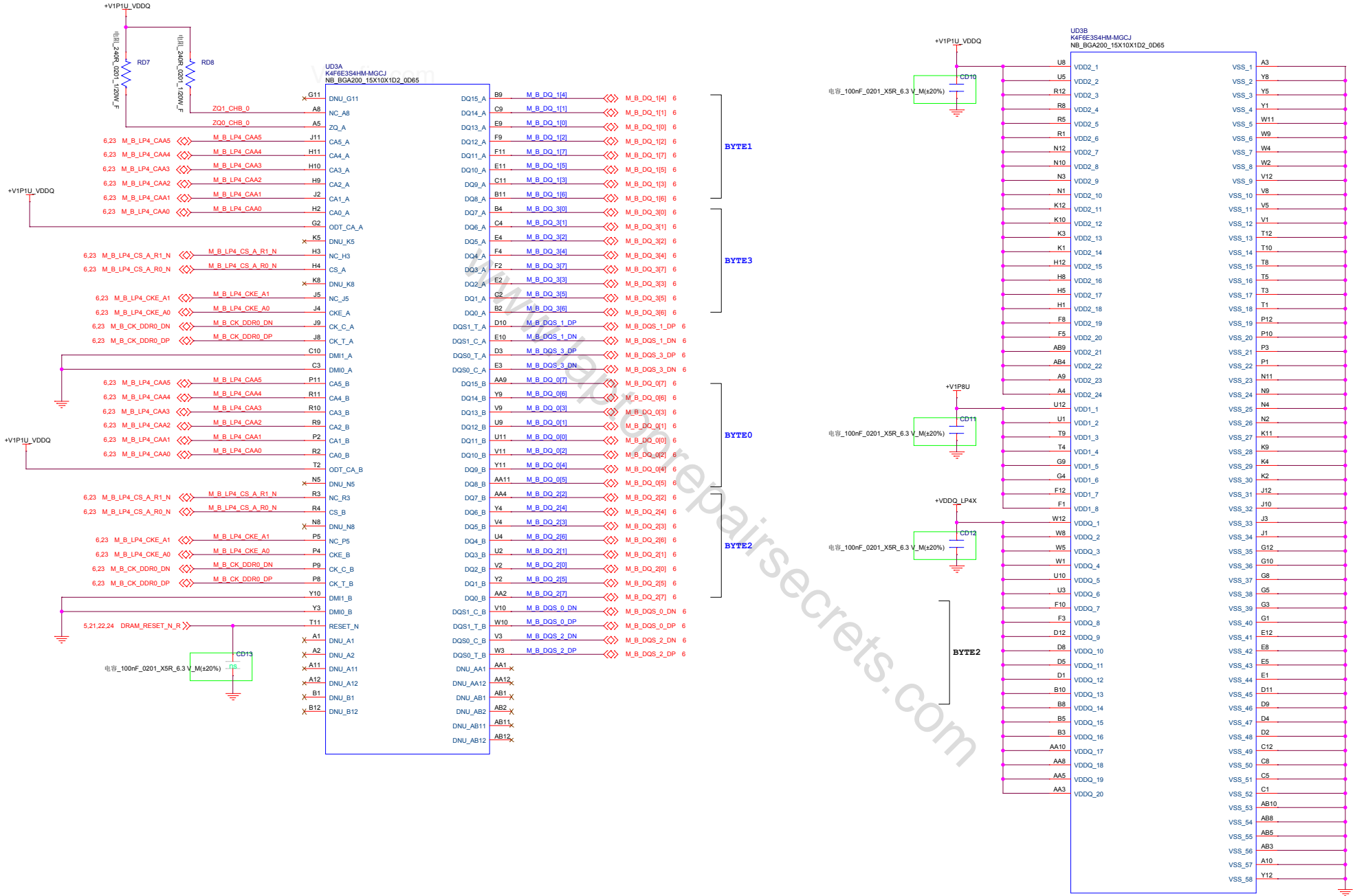
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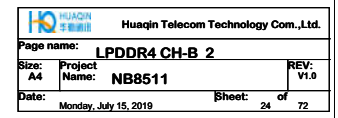
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| Date: <b>Monday, July 15, 2019</b>  |                                | Sheet: <b>20</b>                    | of <b>72</b> |





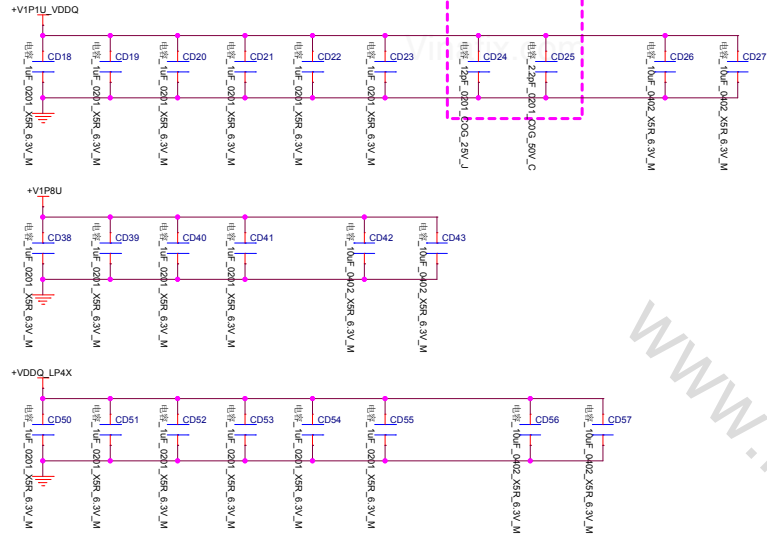




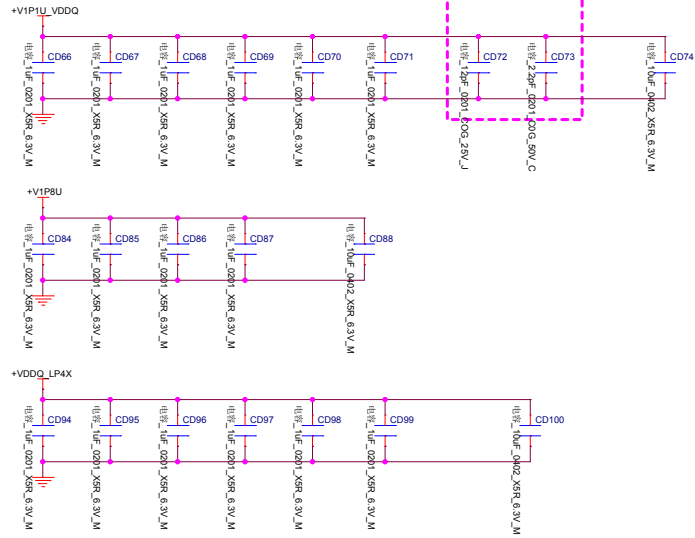


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL A

Place as close as possible to UD?

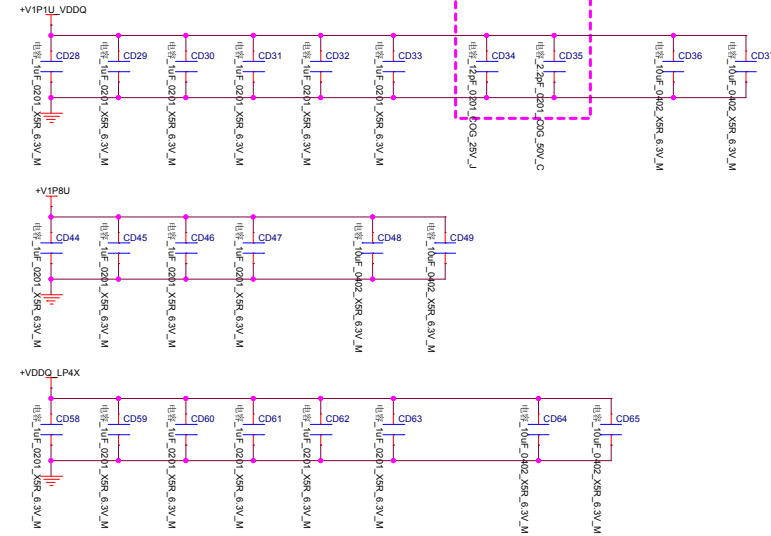


Place as close as possible to UD?

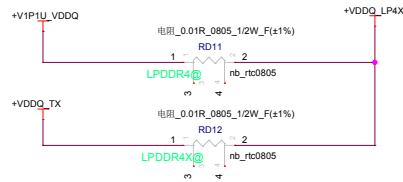
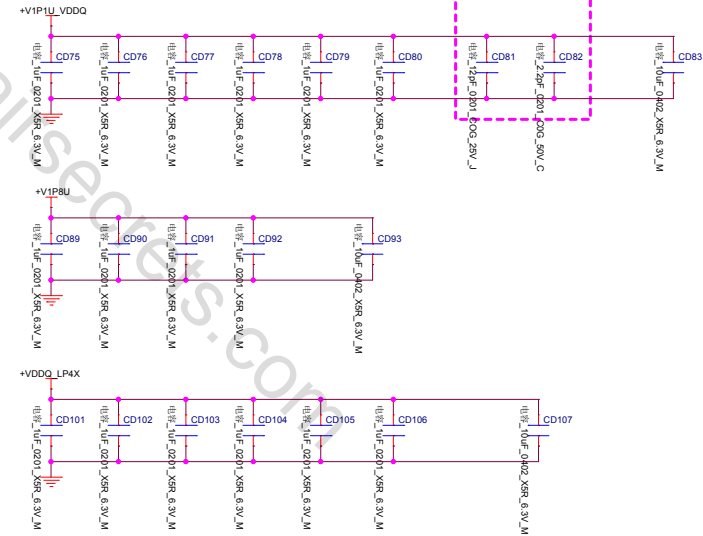


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL B

Place as close as possible to UD?




Place as close as possible to UD?




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|  |                                |                                     |       |
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| Date: Monday, July 15, 2019  |                                | Sheet: 26                           | of 72 |


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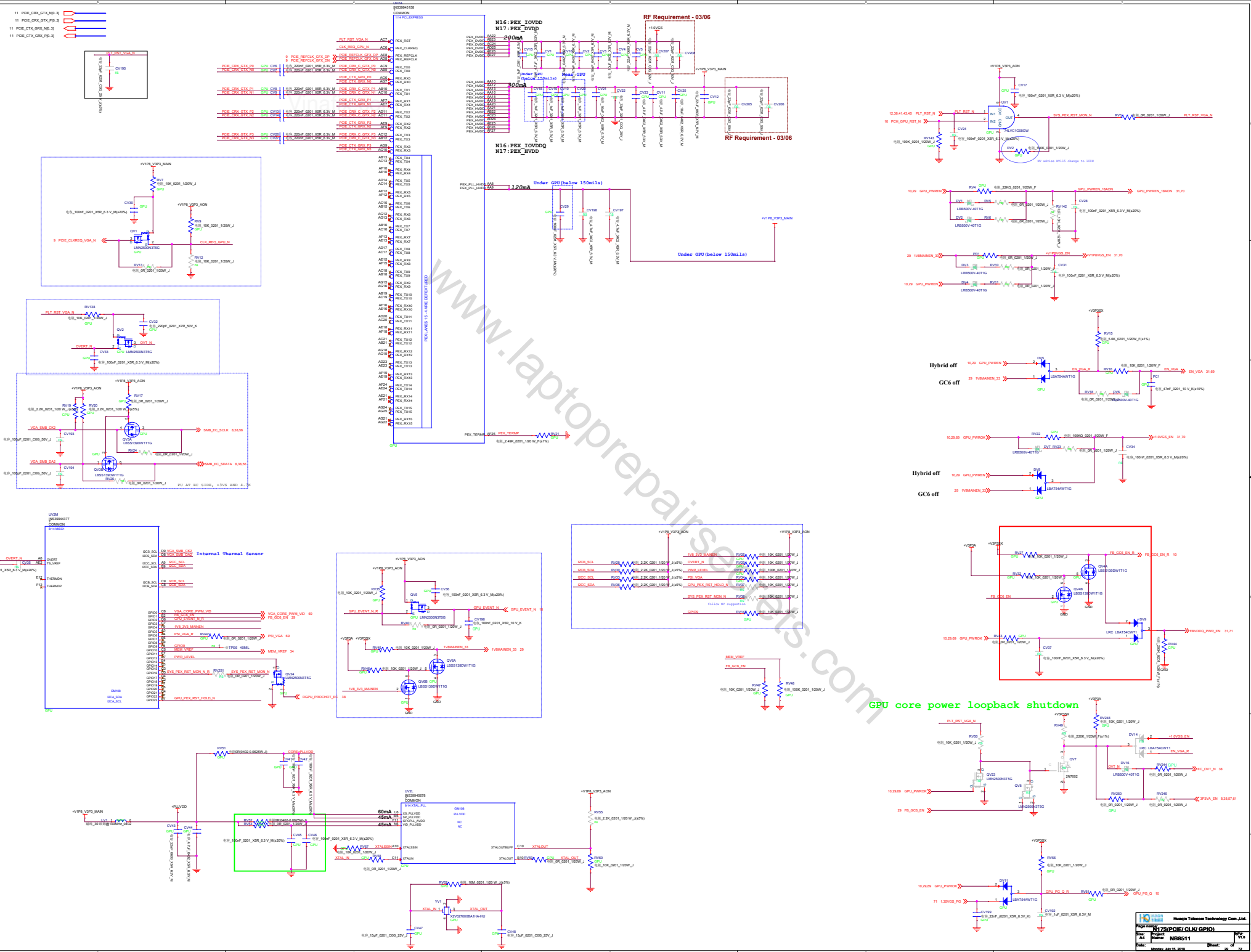
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|  HUAQIN<br>华勤通讯 |                                | Huaqin Telecom Technology Com.,Ltd. |              |
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| Date: <b>Monday, July 15, 2019</b>   |                                | Sheet: <b>27</b> of <b>72</b>       |              |

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| Date: <b>Monday, July 15, 2019</b>  |                                | Sheet: <b>28</b>                    | of <b>72</b> |



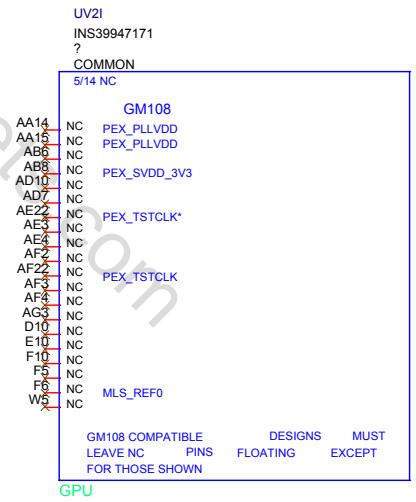
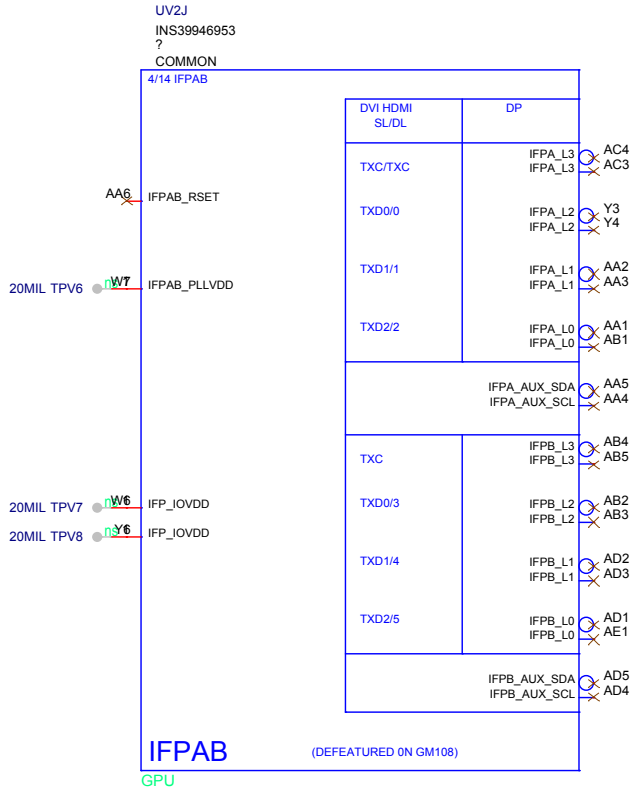
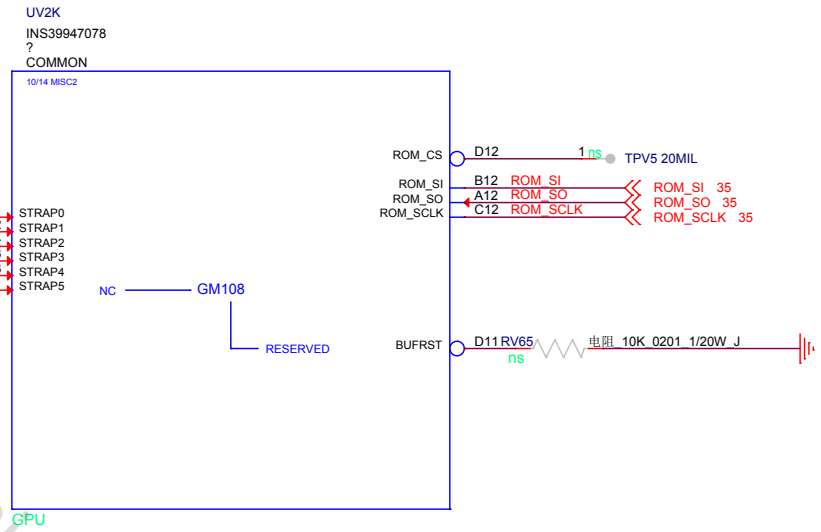
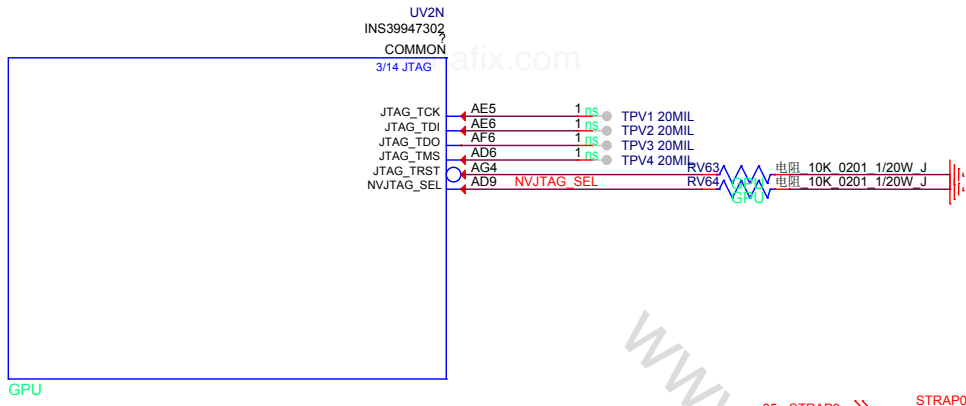




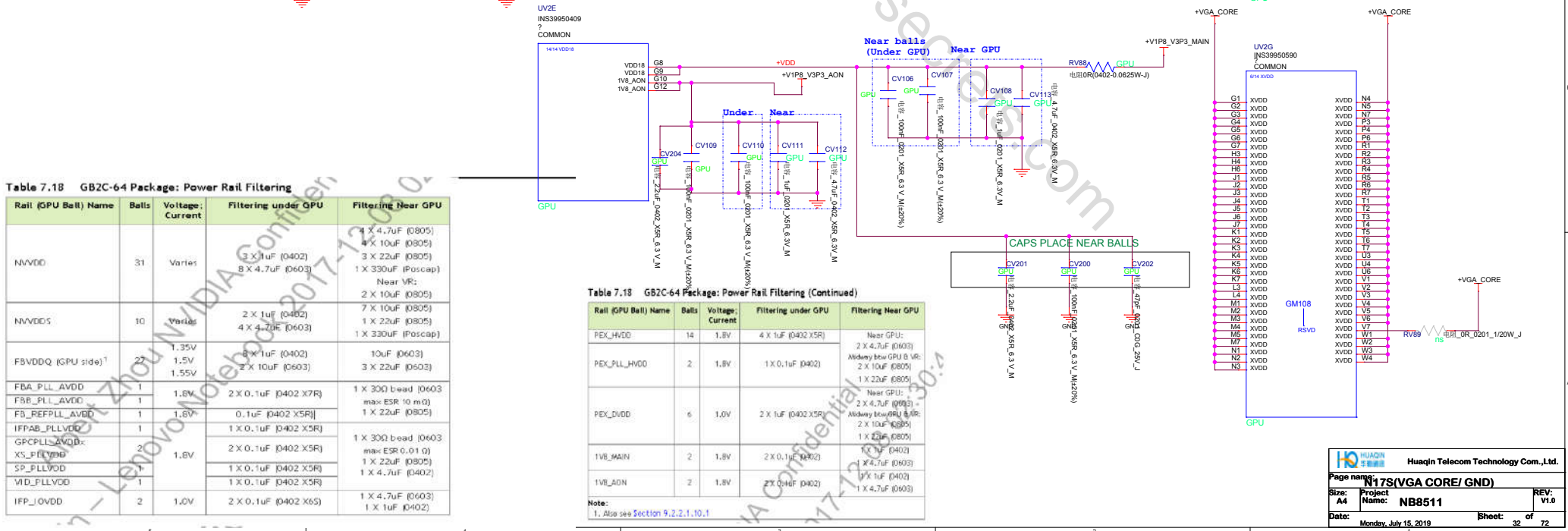
Table 7.18 GB2C-64 Package: Power Rail Filtering

| Rail (GPU Ball) Name           | Balls | Voltage: Current       | Filtering under GPU                | Filtering Near GPU   |
|--------------------------------|-------|------------------------|------------------------------------|--|
| NVDD                           | 31    | Varies                 | 3 X 1uF (0402)<br>8 X 4.7uF (0603) | 1 X 4.7uF (0805)<br>4 X 10uF (0805)<br>3 X 22uF (0805)<br>1 X 330uF (Pocap)<br>Near VR:<br>2 X 10uF (0805) |
| NVDD5                          | 10    | Varies                 | 2 X 1uF (0402)<br>4 X 4.7uF (0603) | 7 X 10uF (0805)<br>1 X 22uF (0805)<br>1 X 330uF (Pocap)  |
| FBVDDQ (GPU side) <sup>1</sup> | 27    | 1.35V<br>1.5V<br>1.55V | 8 X 1uF (0402)<br>2 X 10uF (0603)  | 10uF (0603)<br>3 X 22uF (0603)   |
| FBA_PLL_AVDD                   | 1     | 1.8V                   | 2 X 0.1uF (0402 X7R)               | 1 X 300 bead (0603<br>max<ESR 10 mΩ)   |
| FBB_PLL_AVDD                   | 1     | 1.8V                   | 0.1uF (0402 X5R)                   | 1 X 22uF (0805)  |
| FB_REFPLL_AVDD                 | 1     | 1.8V                   | 1 X 0.1uF (0402 X5R)               | 1 X 22uF (0805)  |
| IFPAB_PLLVDD                   | 1     | 1.8V                   | 1 X 0.1uF (0402 X5R)               | 1 X 300 bead (0603<br>max<ESR 0.01 Ω)  |
| GPCPLL_AVDD                    | 2     | 1.8V                   | 2 X 0.1uF (0402 X5R)               | 1 X 4.7uF (0402)   |
| XS_PLLVDD                      | 1     | 1.8V                   | 1 X 0.1uF (0402 X5R)               | 1 X 4.7uF (0402)   |
| SP_PLLVDD                      | 1     | 1.8V                   | 1 X 0.1uF (0402 X5R)               | 1 X 4.7uF (0402)   |
| WD_PLLVDD                      | 1     | 1.8V                   | 1 X 0.1uF (0402 X5R)               | 1 X 4.7uF (0402)   |
| IFP_OVDD                       | 2     | 1.0V                   | 2 X 0.1uF (0402 X65)               | 1 X 4.7uF (0402)<br>1 X 1uF (0402)   |

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

| Rail (GPU Ball) Name | Balls | Voltage: Current | Filtering under GPU | Filtering Near GPU  |
|----------------------|-------|------------------|---------------------|---|
| PEX_HVDD             | 14    | 1.8V             | 4 X 1uF (0402 X5R)  | Near GPU:<br>2 X 4.7uF (0603)<br>Midway bet GPU & VR:<br>2 X 10uF (0805)<br>1 X 22uF (0805) |
| PEX_PLL_HVDD         | 2     | 1.8V             | 1 X 0.1uF (0402)    | Near GPU:<br>2 X 4.7uF (0603)<br>Midway bet GPU & VR:<br>2 X 10uF (0805)<br>1 X 22uF (0805) |
| PEX_DVDD             | 6     | 1.0V             | 2 X 1uF (0402 X5R)  | Near GPU:<br>2 X 4.7uF (0603)<br>Midway bet GPU & VR:<br>2 X 10uF (0805)<br>1 X 22uF (0805) |
| 1V8_MAIN             | 2     | 1.8V             | 2 X 0.1uF (0402)    | 1 X 1uF (0402)<br>1 X 4.7uF (0603)  |
| 1V8_AON              | 2     | 1.8V             | 2 X 0.1uF (0402)    | 1 X 1uF (0402)<br>1 X 4.7uF (0603)  |

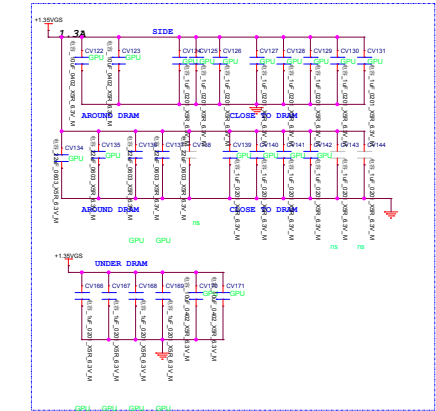
Note:  
1. Also see Section 9.2.2.1.10.1



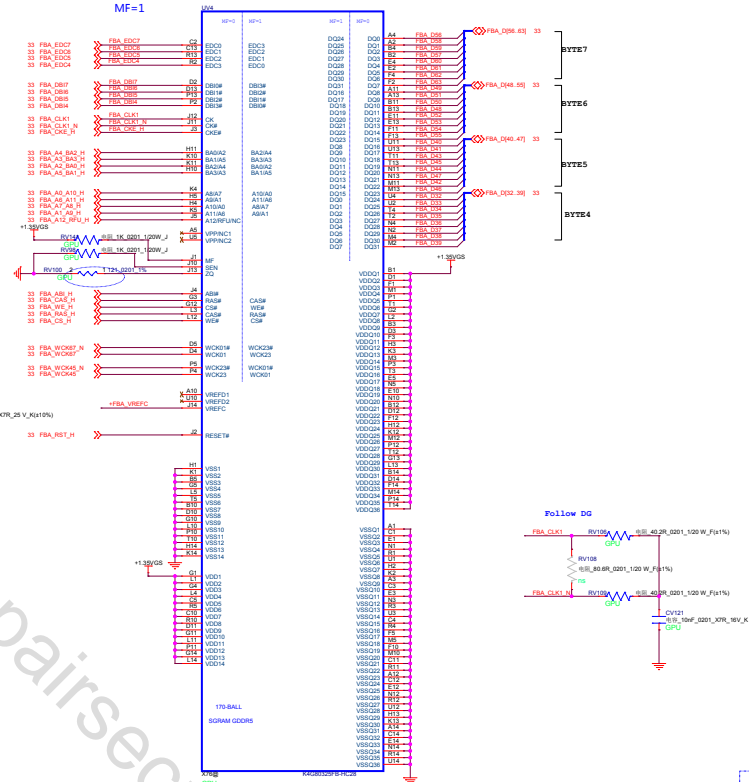




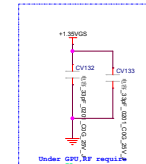
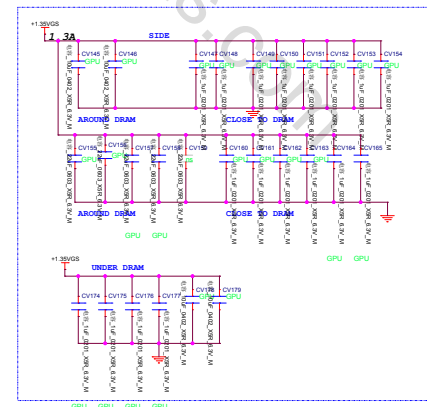
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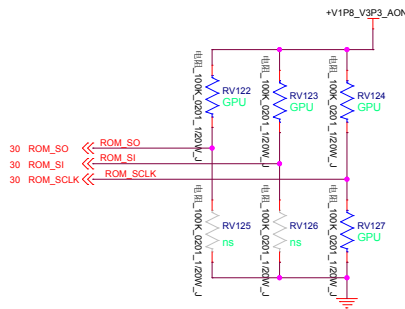
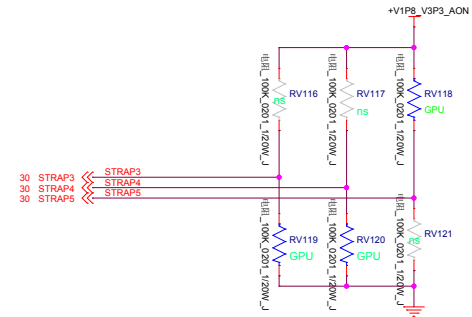
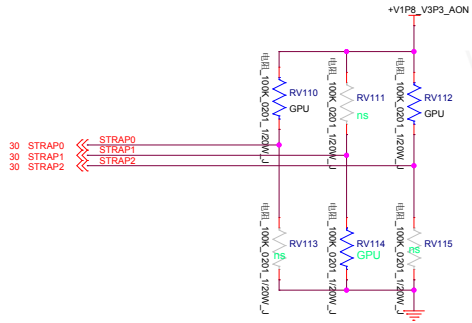


MF=1



| Decoupling Capacitors              |             | Recommended Quantity and Placement (per DRAM device) |  |
|------------------------------------|-------------|--|--|
| Capacitance                        | Type [Size] | Quantity   | Placement (by DRAM Interface Mode)   |
| <b>Combined FBVDD-FBVDQ/Q Rail</b> |             |  |  |
| 1.0 uF                             | X65 [0402]  | 10   | For x32 DRAM: Under the DRAM FBVDD or FBVDQ/Q ball   |
| 10 uF                              | X65 [0603]  | 4  | For x16 DRAM in a "clamshell" PCB configuration: As close to DRAM periphery as possible.<br><br>Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.   |
| 1.0 uF                             | X65 [0402]  | 8 additional   | For x32 DRAM: Close x32 interface to drive main POK DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDQ/Q ball via if possible. See <a href="#">Figure 9-23</a> for an example. |
| 10 uF                              | X65 [0603]  | 2  | Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.  |
| 22 uF                              | X65 [0603]  | 5  | For 4 GHz WCK (8 Gbps data rates):<br>Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.  |





For N17

| GPU        | Vendor  | Manufacturer       | Strap | Strap2 | Strap1 | Strap0 |
|------------|---------|--------------------|-------|--------|--------|--------|
| N17S-G1    | Samsung | K4G80325FB-HC28    | 0x0   | L      | L      | L      |
|            | Micron  | MT51J256M32HF-70:A | 0x1   | L      | L      | H      |
|            | Hynix   | H5GC8H24MJR-ROC    | 0x2   | L      | H      | L      |
|            | Micron  | MT51J256M32HF-70:B | 0x4   | H      | L      | L      |
| N17S_G0/G2 | Hynix   | H5GC8H24AJR-ROC    | 0x5   | H      | L      | H      |
|            | Micron  | MT51J256M32HF-80:B | 0x9   | L      | M      | L      |
|            | Hynix   | H5GC8H24AJR-R2C    | 0xA   | L      | M      | H      |

| PN            | MPN             | STRAP | Vendor  |
|---------------|-----------------|-------|---------|
| HQ11121499000 | K4G80325FB-HC28 | 0x00  | Samsung |
| HQ11121497000 | H5GC8H24MJR-R4C | 0x02  | Hynix   |

| Physical Strapping pin | Power Rail | RAM_CFG[3] | RAM_CFG[0x02] | RAM_CFG[1] | RAM_CFG[0x00] |
|------------------------|------------|------------|---------------|------------|---------------|
| STRAP0                 |            | L          |               |            | L             |
| STRAP1                 |            | H          |               |            | L             |
| STRAP2                 |            | L          |               |            | L             |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |
|                        |            |            |               |            |               |

| SMBUS | ALT | ADDR                   |
|-------|-----|------------------------|
| 0     |     | 0x9E (Default)         |
| 1     |     | 0x9C (Multi-GPU usage) |

| DEVID | SEL       |
|-------|-----------|
| 0     | (Default) |
| 1     |           |

| PCIE | CFG       |
|------|-----------|
| 0    | (Default) |
| 1    |           |

| VGA | DEVICE                      |
|-----|-----------------------------|
| 0   | 3D Device (Class Code 302h) |
| 1   | VGA Device (Default)        |

| Physical Strapping pin | Power Rail | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
|------------------------|------------|--------------|--------------|--------------|--------------|
| ROM_SCLK               | M          |              |              |              |              |
| ROM_SI                 | H          | Disable      | Disable      | Disable      | Disable      |
| ROM_SO                 | H          |              |              |              |              |

Table 5.3 RAMCFG

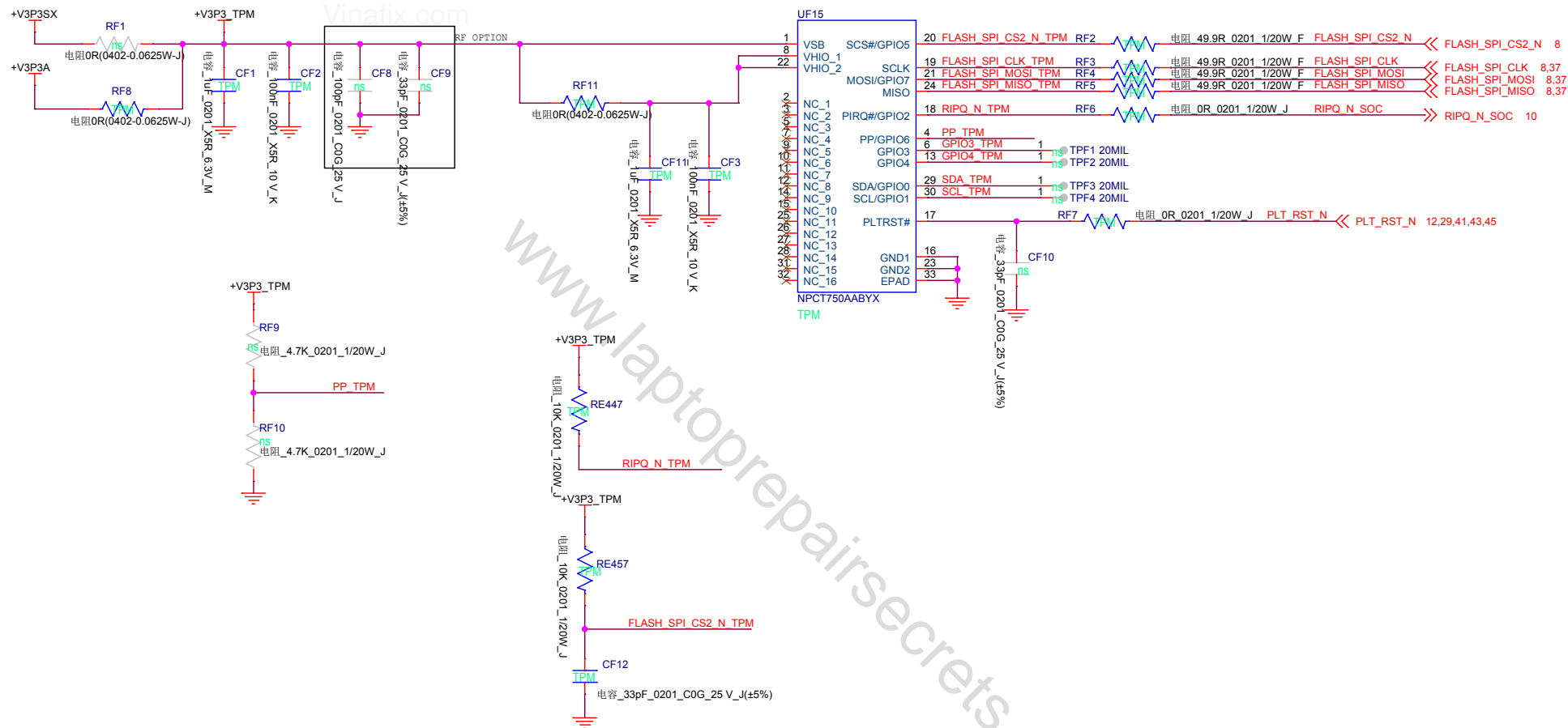
| Strap Pins <small>see Note</small> |        |        | RAMCFG Setting Number  |
|------------------------------------|--------|--------|--|
| STRAP2                             | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers) |
| L                                  | L      | L      | 0 (0x0000)   |
| L                                  | L      | H      | 1 (0x0001)   |
| L                                  | H      | L      | 2 (0x0002)   |
| L                                  | H      | H      | 3 (0x0003)   |
| H                                  | L      | L      | 4 (0x0004)   |
| H                                  | L      | H      | 5 (0x0005)   |
| H                                  | H      | L      | 6 (0x0006)   |
| H                                  | H      | H      | 7 (0x0007)   |
| L                                  | L      | M      | 8 (0x0008)   |
| L                                  | M      | L      | 9 (0x0009)   |
| L                                  | M      | H      | 10 (0x000A)  |
| L                                  | H      | M      | 11 (0x000B)  |
| M                                  | L      | L      | 12 (0x000C)  |
| M                                  | L      | H      | 13 (0x000D)  |

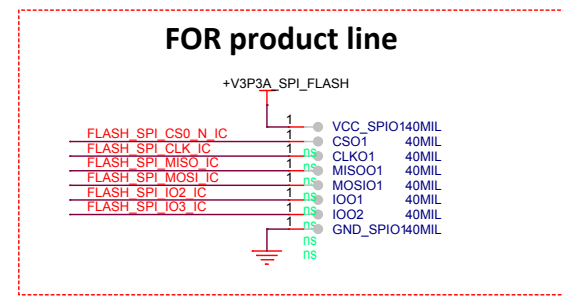
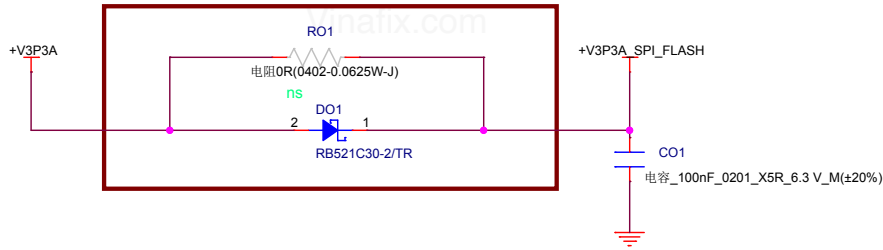
Table 5. N17S-G0/G2 GDDR5 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert | Qual Plan | Status           |
|----------------|------------------------------|---------|--------|--------------------------|--------------|-------|--------------------|-----------------|-----------|------------------|
| 8 Gb           | 256Mx32 512Mx16              | 1.35V   | Micron | MT51J256M32HF-80:B       | B-die        | 0x9   | 8 Gbps             | N/A             | Full      | Production ready |
|                |                              |         | Hynix  | H5GC8H24AJR-R2C          | A-die        | 0xA   | 8 Gbps             | N/A             | Full      | Production ready |

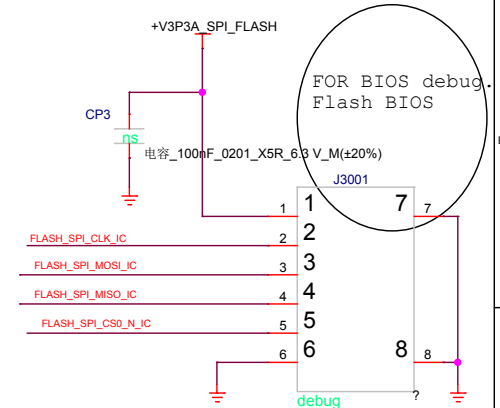
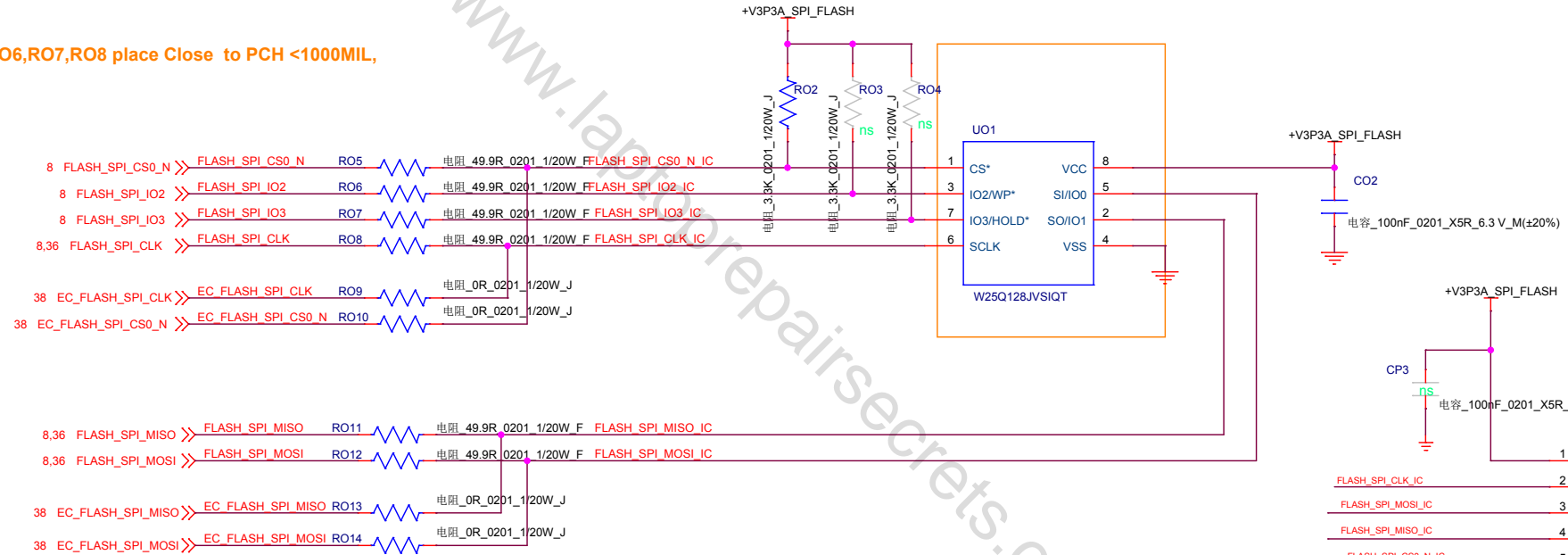
Notes:

- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.



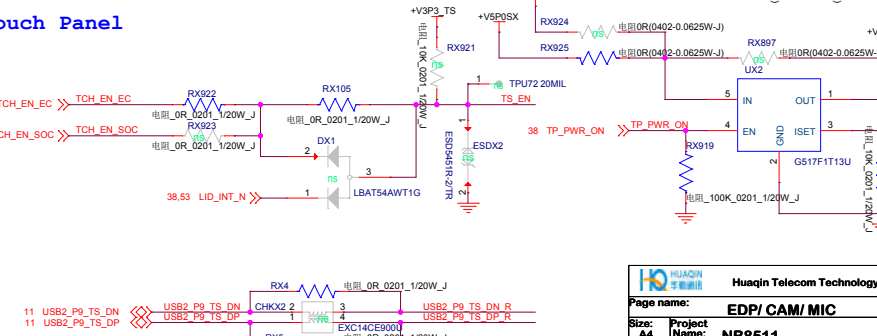
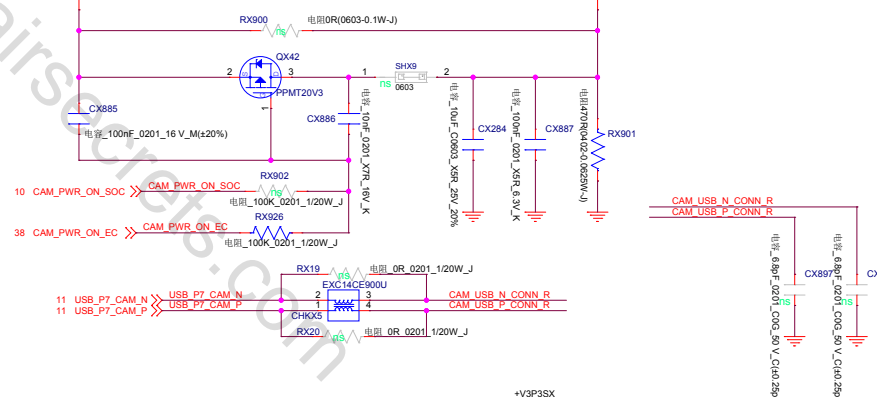
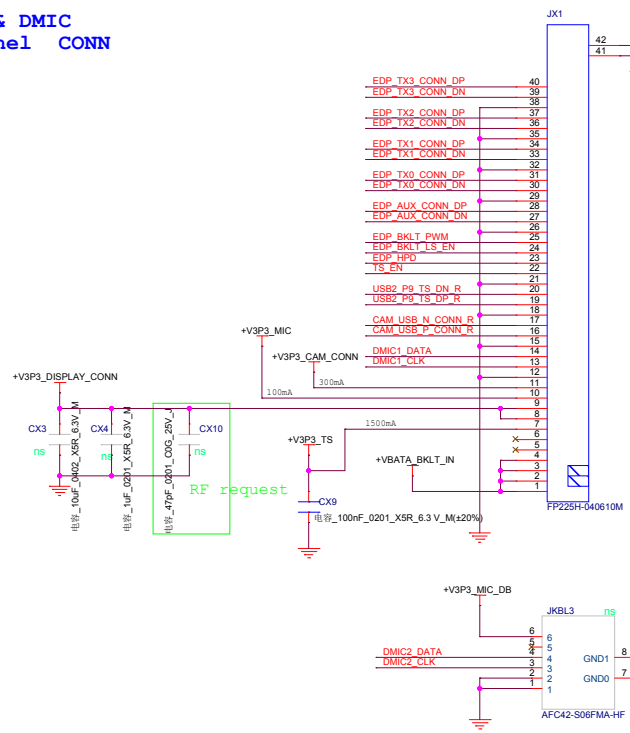
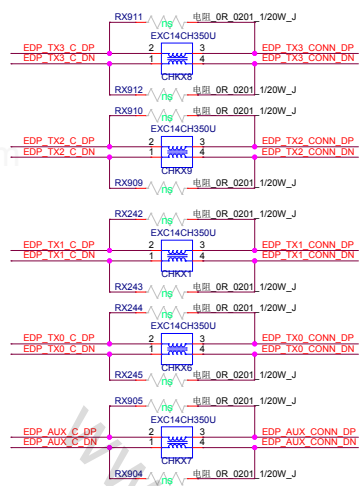


Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,



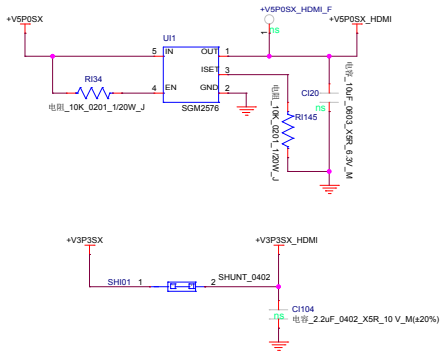


|   |                |     |                |       |                              |              |
|---|----------------|-----|----------------|-------|------------------------------|--------------|
| 7 | EDP_TX3_SOC_DP | >>> | EDP_TX3_SOC_DP | CX890 | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX3_C_DP |
| 7 | EDP_TX3_SOC_DN | >>> | EDP_TX3_SOC_DN | CX890 | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX3_C_DN |
| 7 | EDP_TX2_SOC_DP | >>> | EDP_TX2_SOC_DP | CX890 | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX2_C_DP |
| 7 | EDP_TX2_SOC_DN | >>> | EDP_TX2_SOC_DN | CX890 | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX2_C_DN |
| 7 | EDP_TX1_SOC_DP | >>> | EDP_TX1_SOC_DP | CX1   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX1_C_DP |
| 7 | EDP_TX1_SOC_DN | >>> | EDP_TX1_SOC_DN | CX2   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX1_C_DN |
| 7 | EDP_TX0_SOC_DP | >>> | EDP_TX0_SOC_DP | CX5   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX0_C_DP |
| 7 | EDP_TX0_SOC_DN | >>> | EDP_TX0_SOC_DN | CX6   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_TX0_C_DN |
| 7 | EDP_AUX_SOC_DP | >>> | EDP_AUX_SOC_DP | CX7   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_AUX_C_DP |
| 7 | EDP_AUX_SOC_DN | >>> | EDP_AUX_SOC_DN | CX8   | 电容 100nF 0201 X5R 6.3V M±20% | EDP_AUX_C_DN |

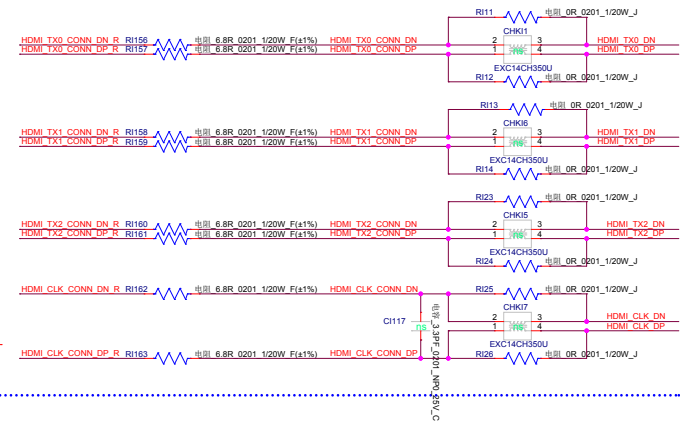
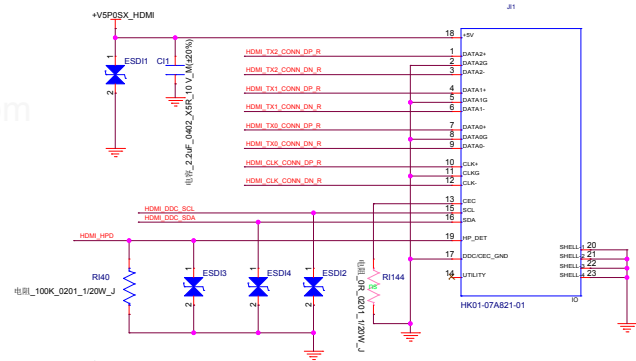




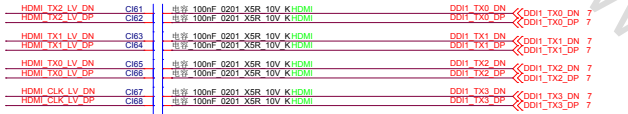
Power 1



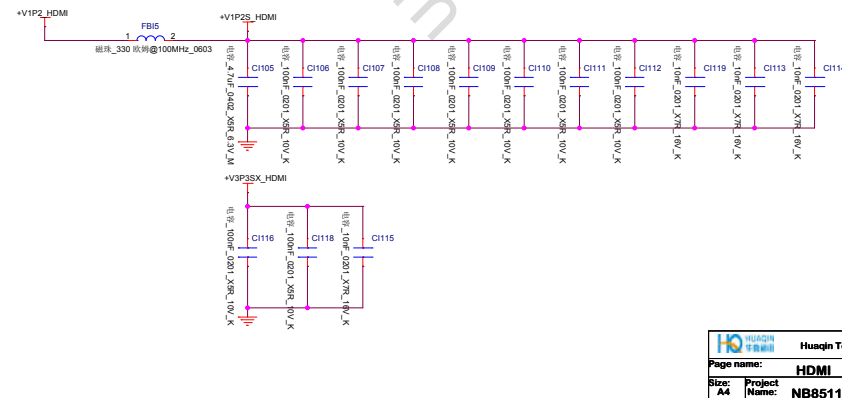
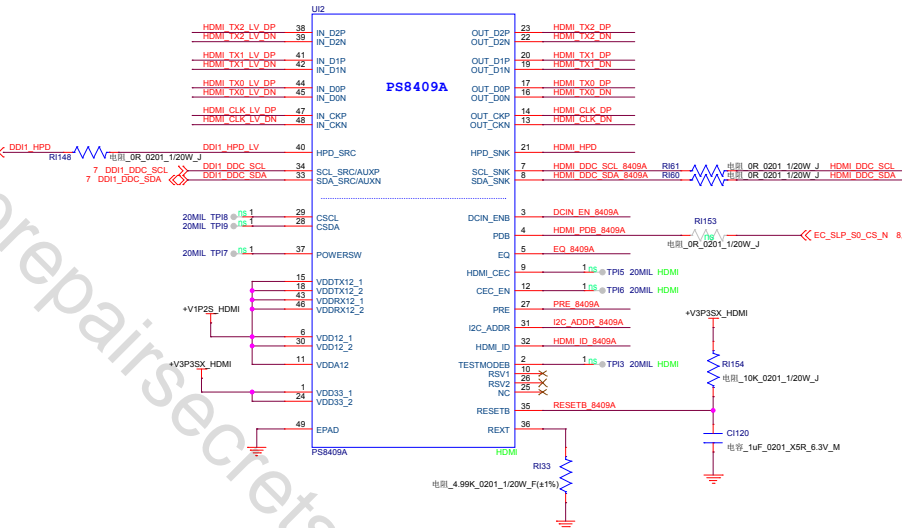
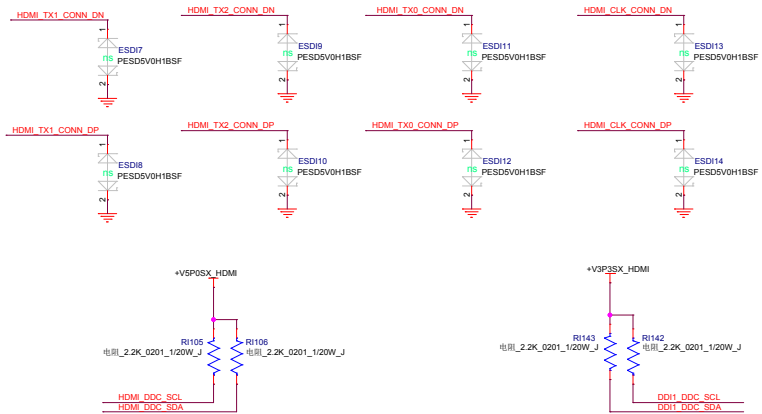
## HDMI CONN



## Signal

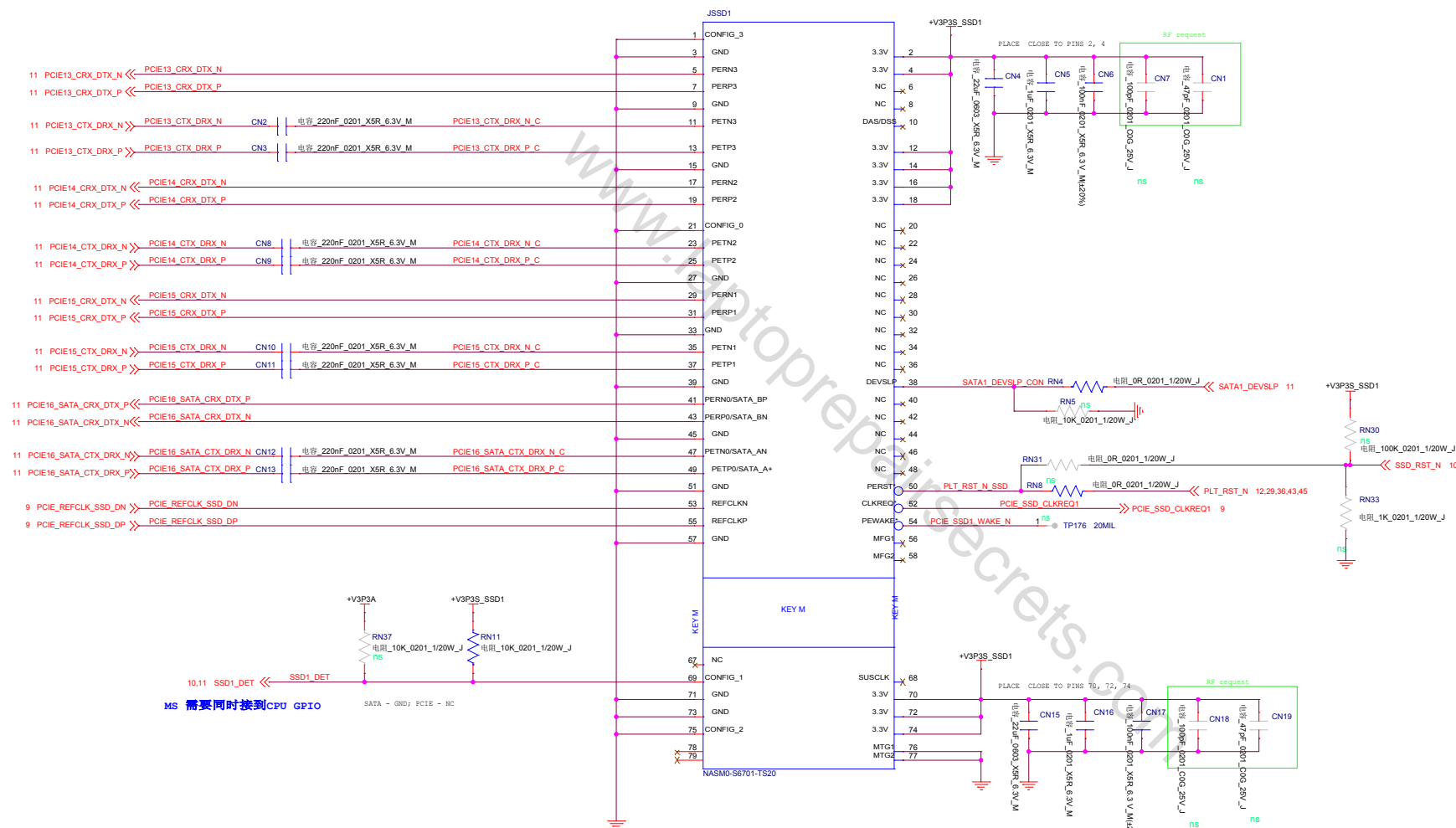


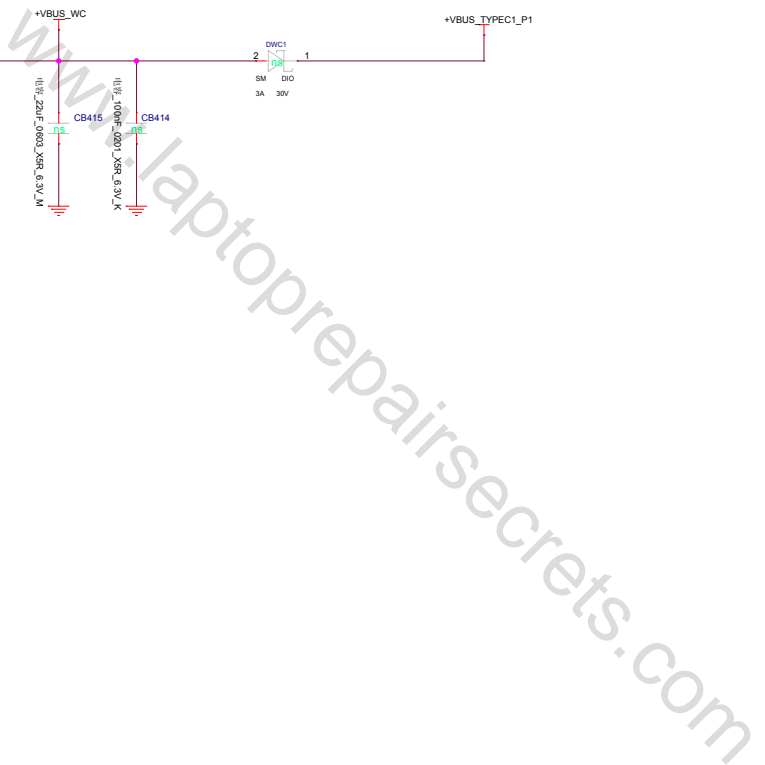
ESD

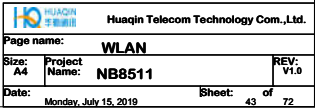




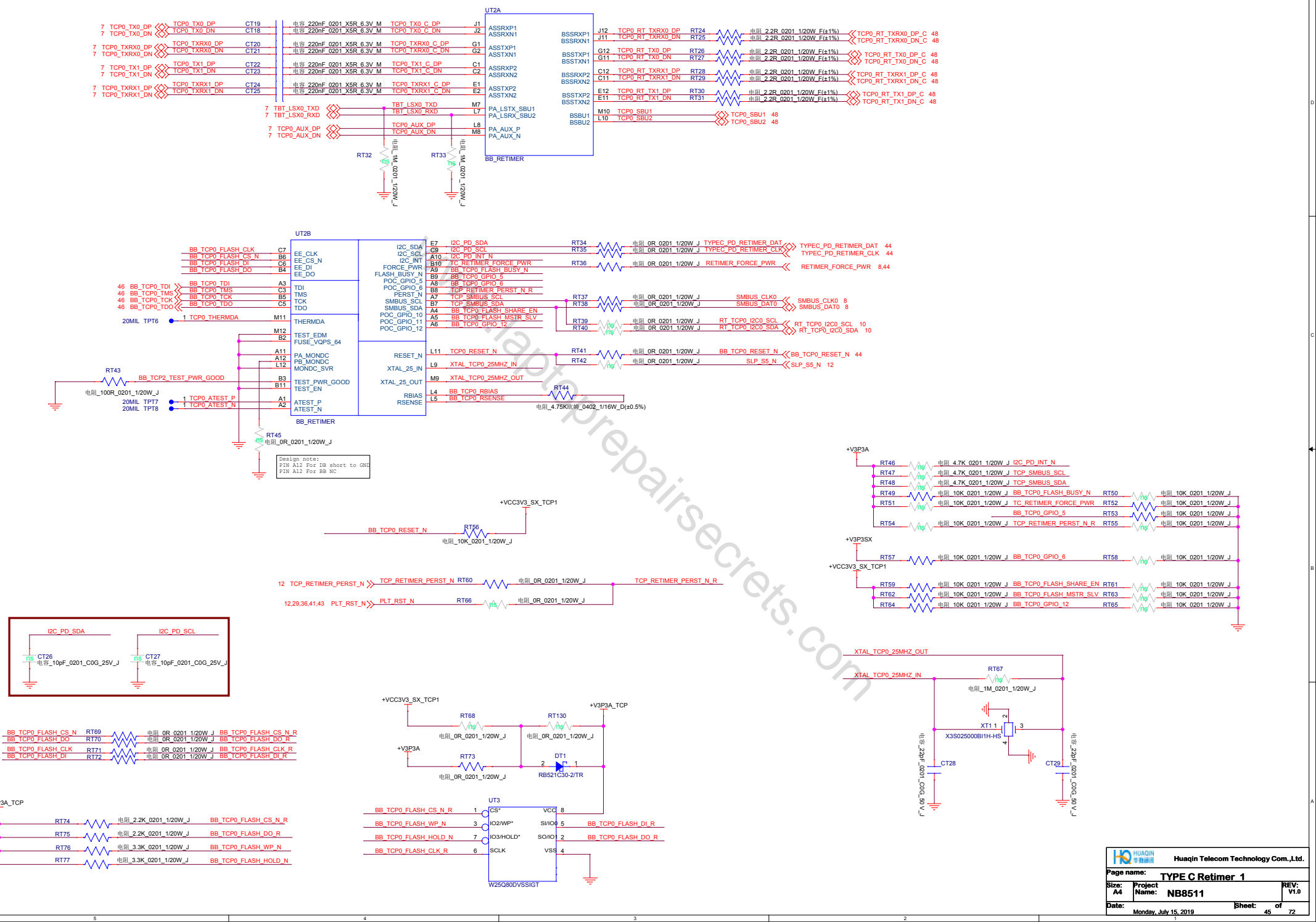
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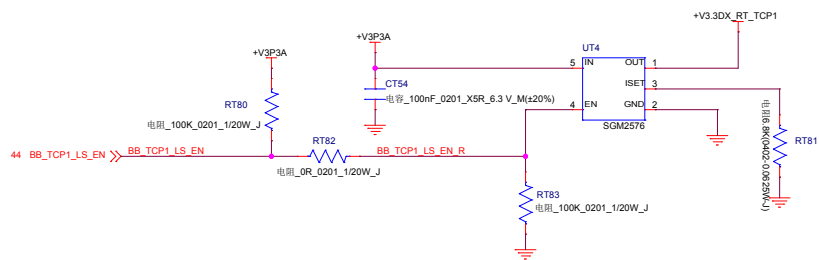
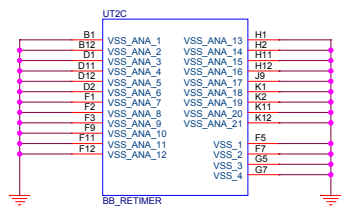
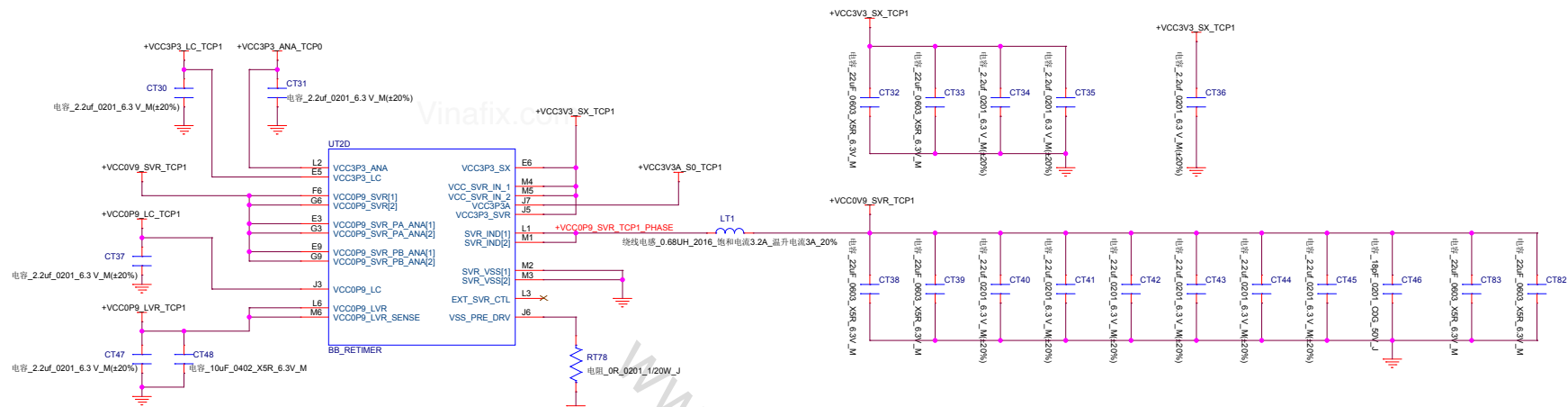




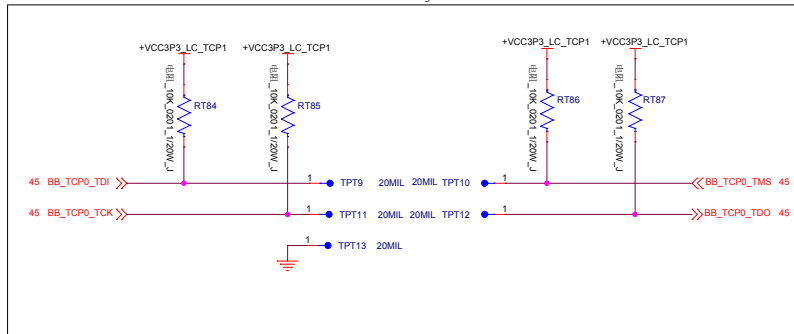




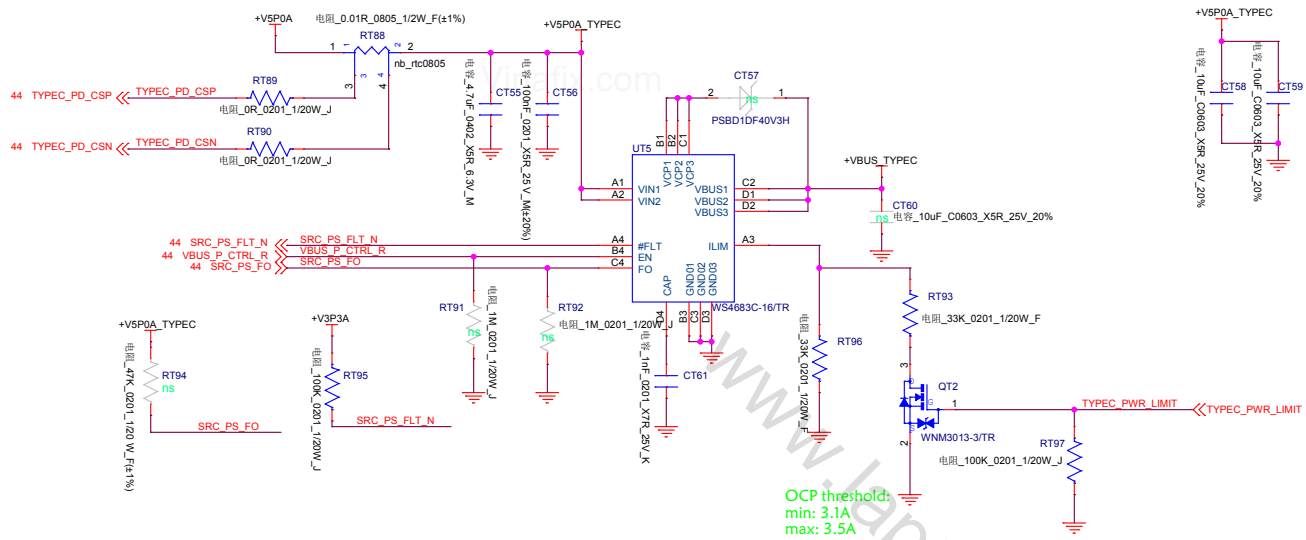




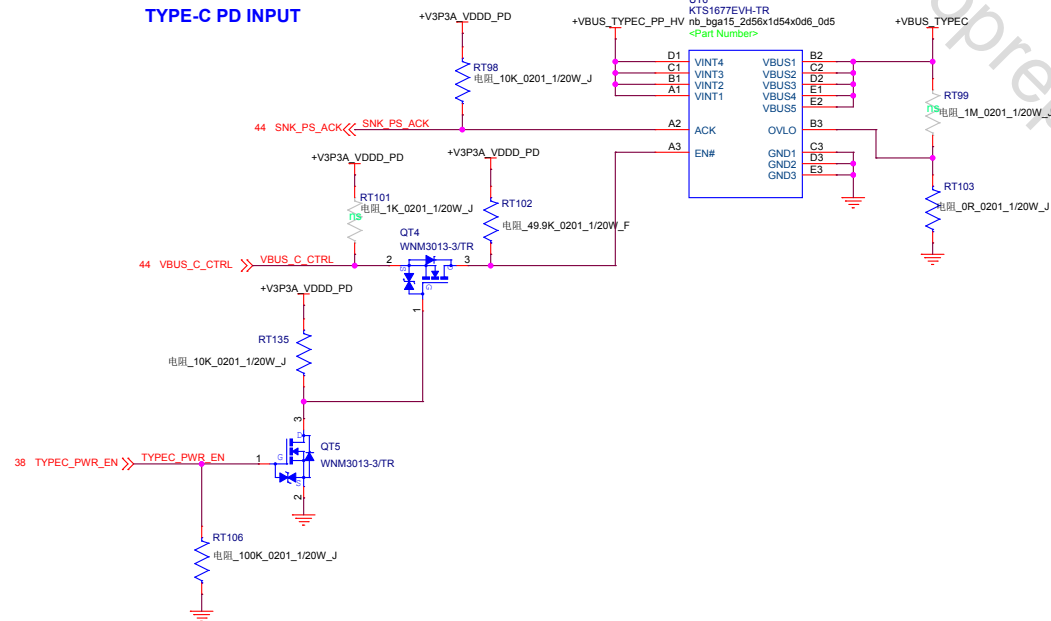
Place together



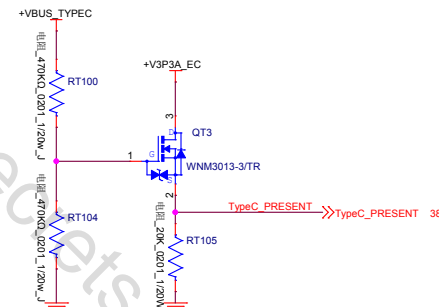
## TYPE-C PD OUTPUT



## TYPE-C PD INPUT

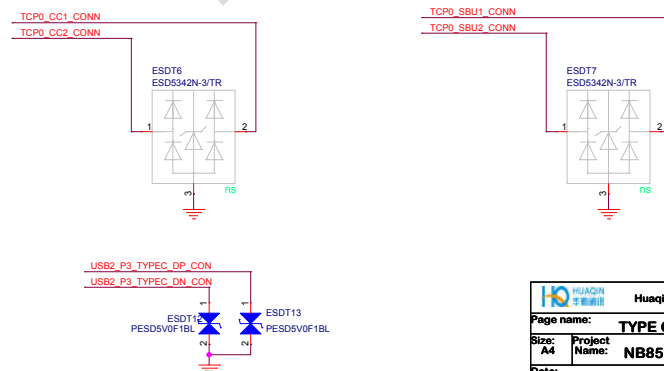
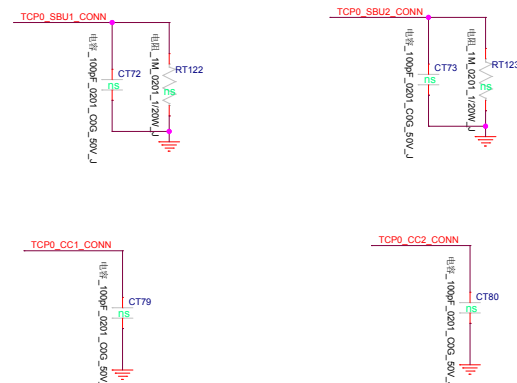
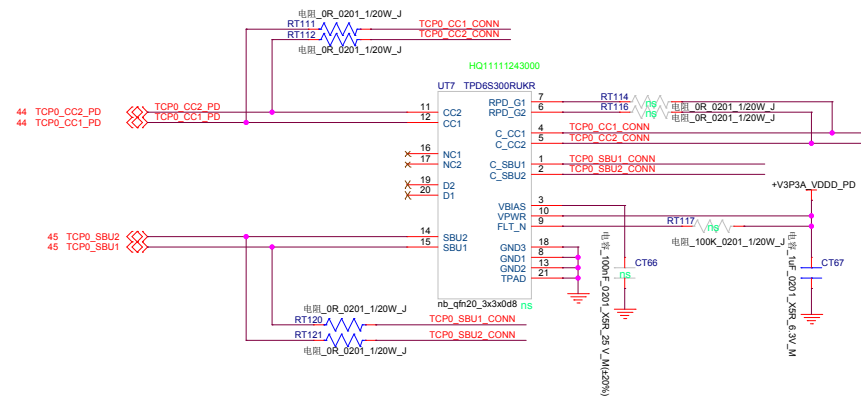


## TYPE-C IN detect



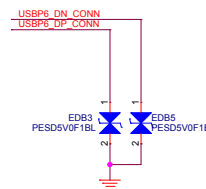
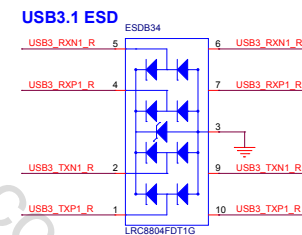
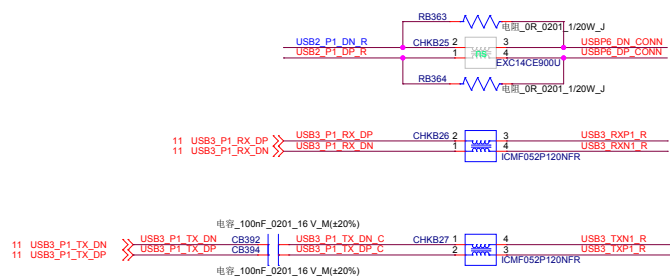
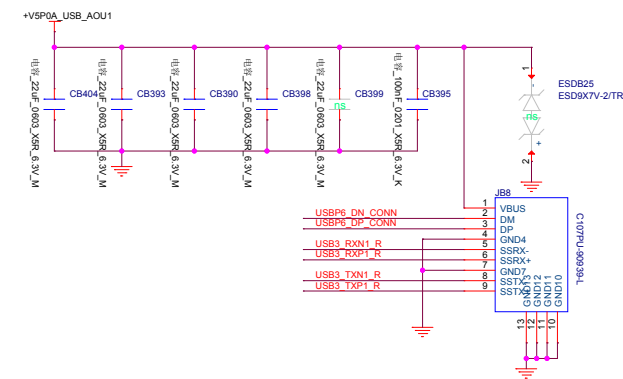
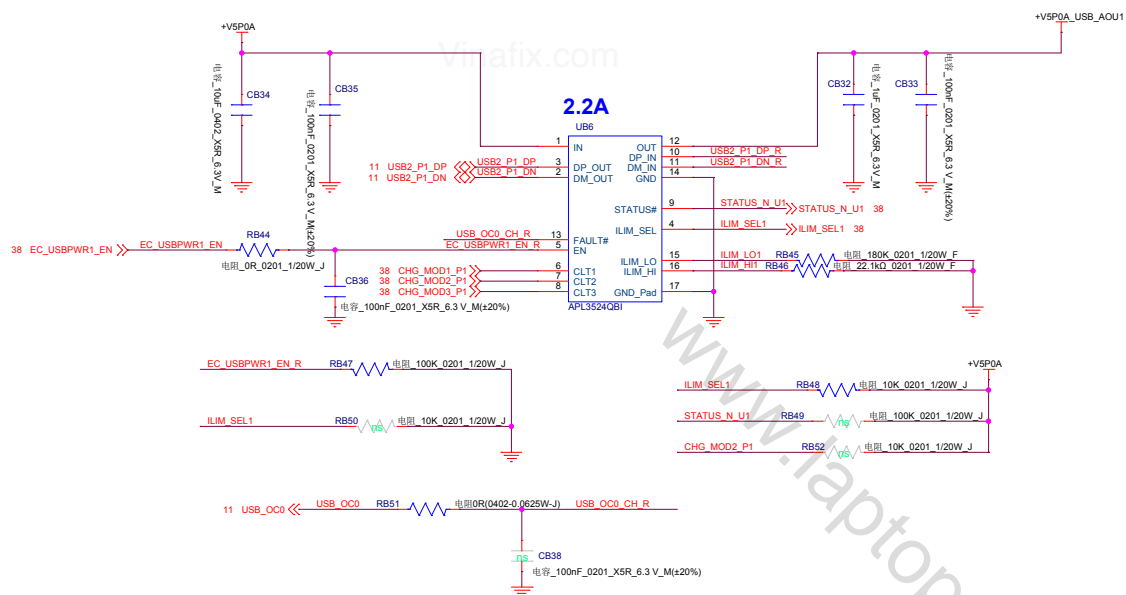
## dead battery power on logic

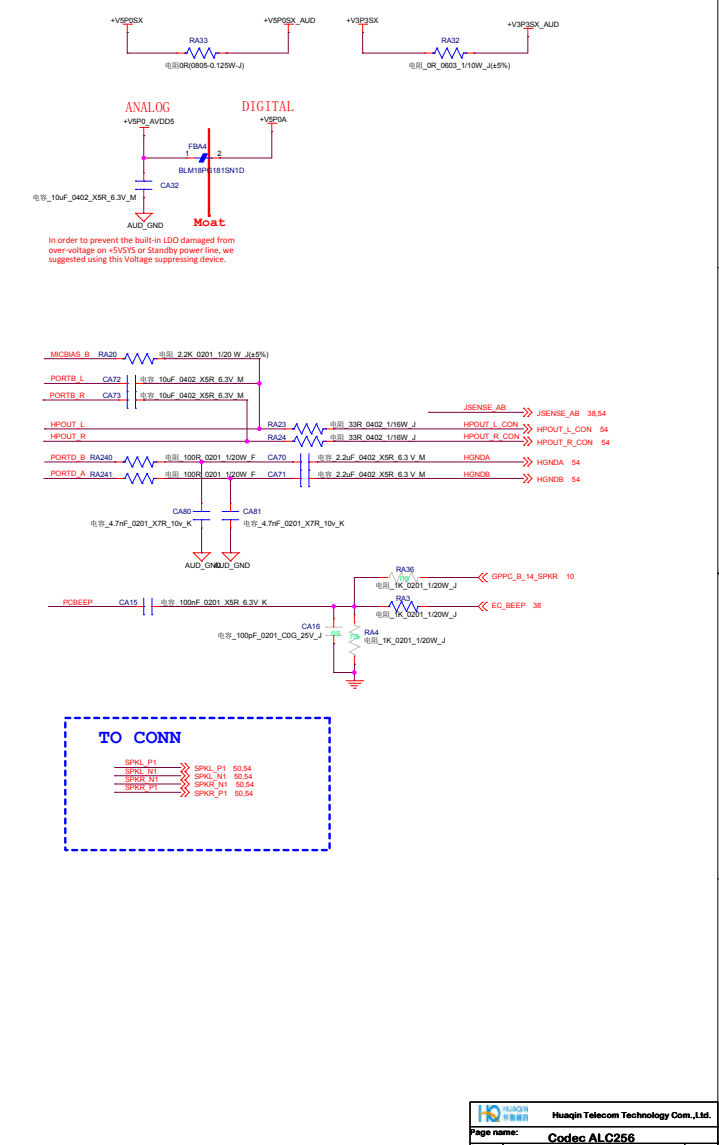
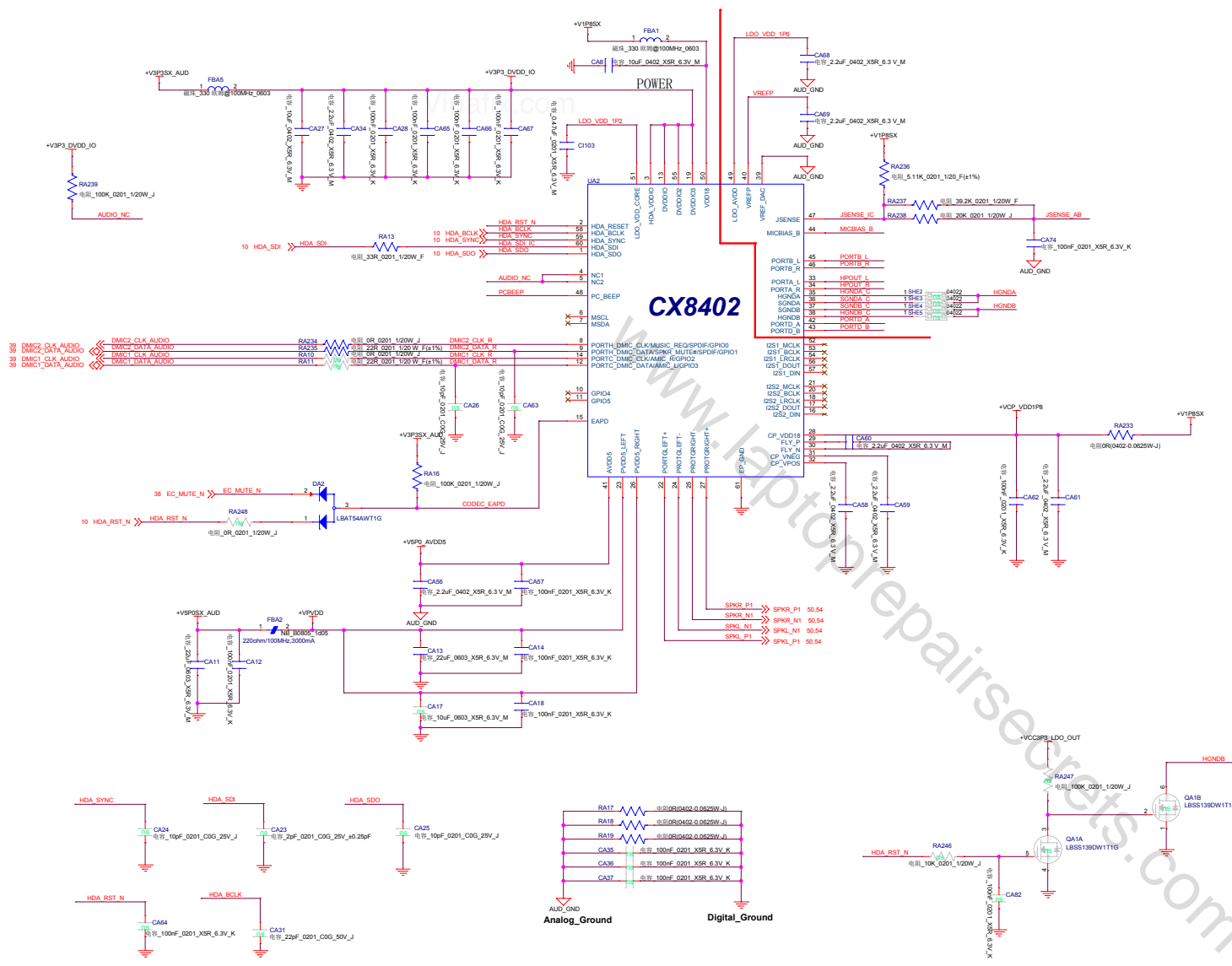
## Discharge



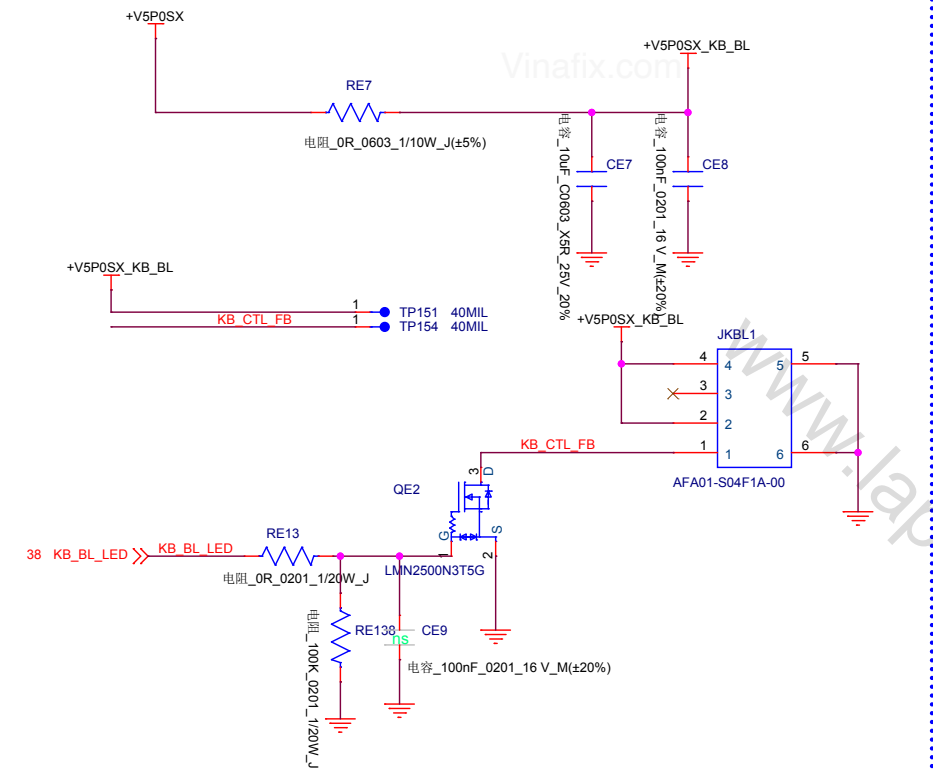


### USB3.1 Signal

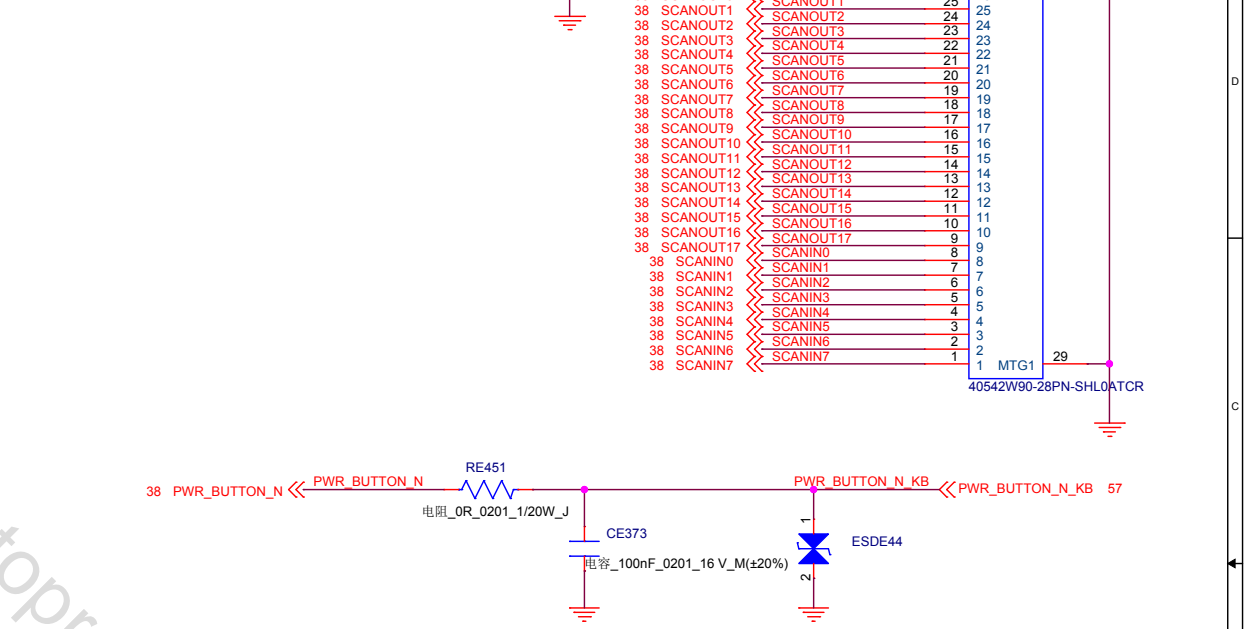




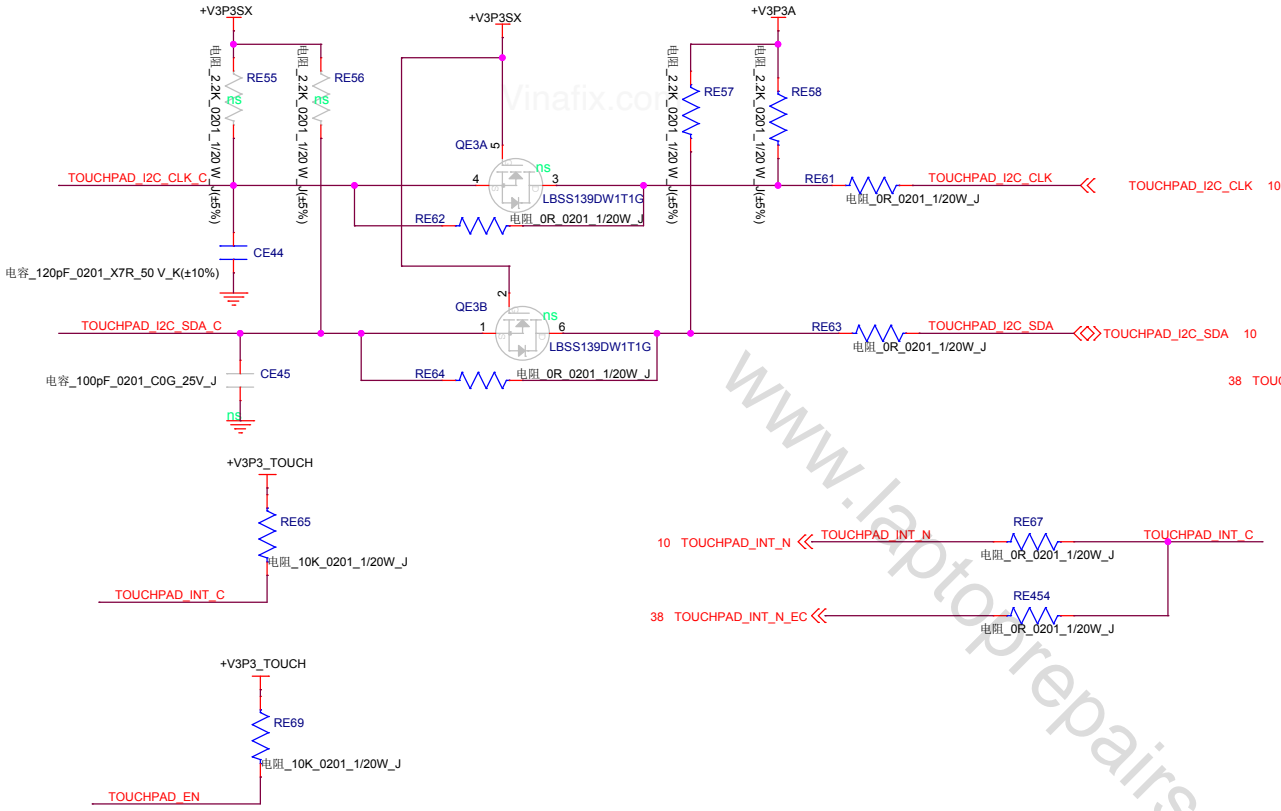
KB Backlight



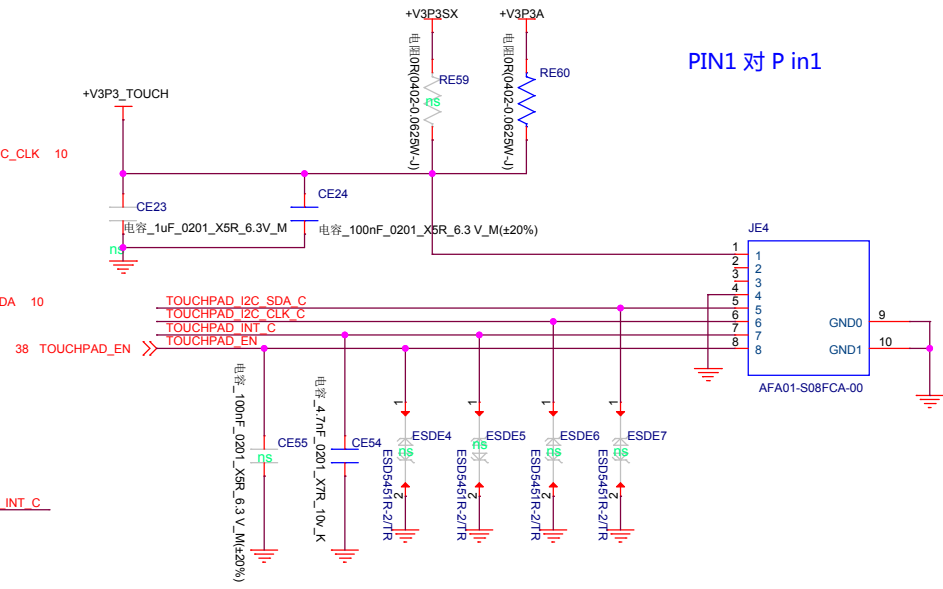
KB CONN



Touch Pad



Touch Pad CONN

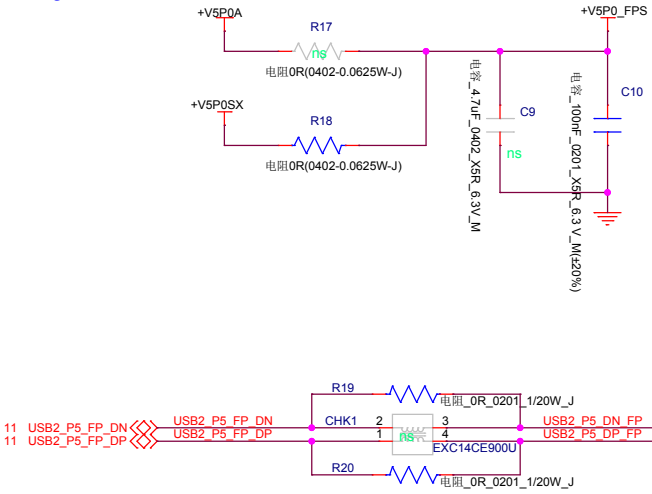


PIN1 对 P in1

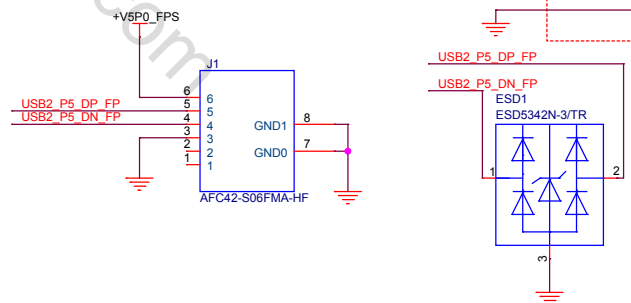
FOR product line

|                   |      |       |       |
|-------------------|------|-------|-------|
| TOUCHPAD_I2C_CLK1 | 1 nS | TP143 | 40MIL |
| TOUCHPAD_I2C_SDA1 | 1 nS | TP142 | 40MIL |
| TOUCHPAD_INT_C    | 1 nS | TP149 | 40MIL |
| TOUCHPAD_EN       | 1 nS | TP150 | 40MIL |
|                   | 1 nS | TP141 | 40MIL |
|                   | 1 nS | TP144 | 40MIL |

Finger Print



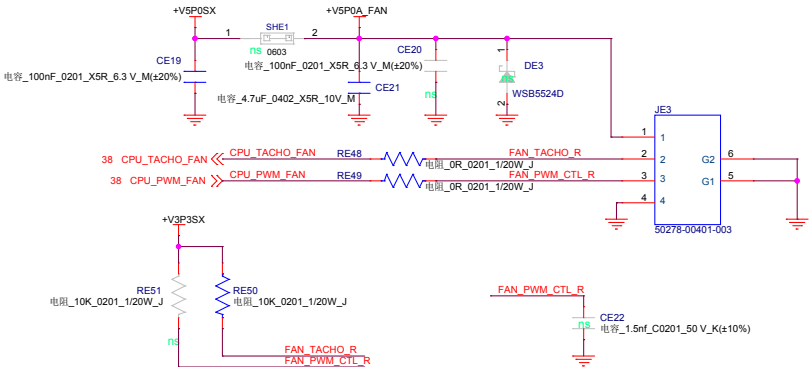
Finger Print CONN



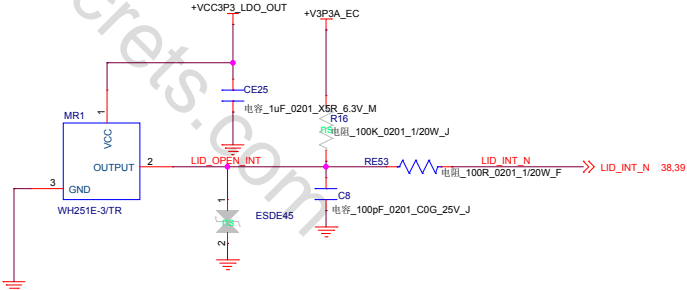
FOR product line

|               |      |       |       |
|---------------|------|-------|-------|
| USB2_P5_DP_FP | 1 nS | TP147 | 40MIL |
| USB2_P5_DN_FP | 1 nS | TP146 | 40MIL |
|               | 1 nS | TP145 | 40MIL |
|               | 1 nS | TP148 | 40MIL |

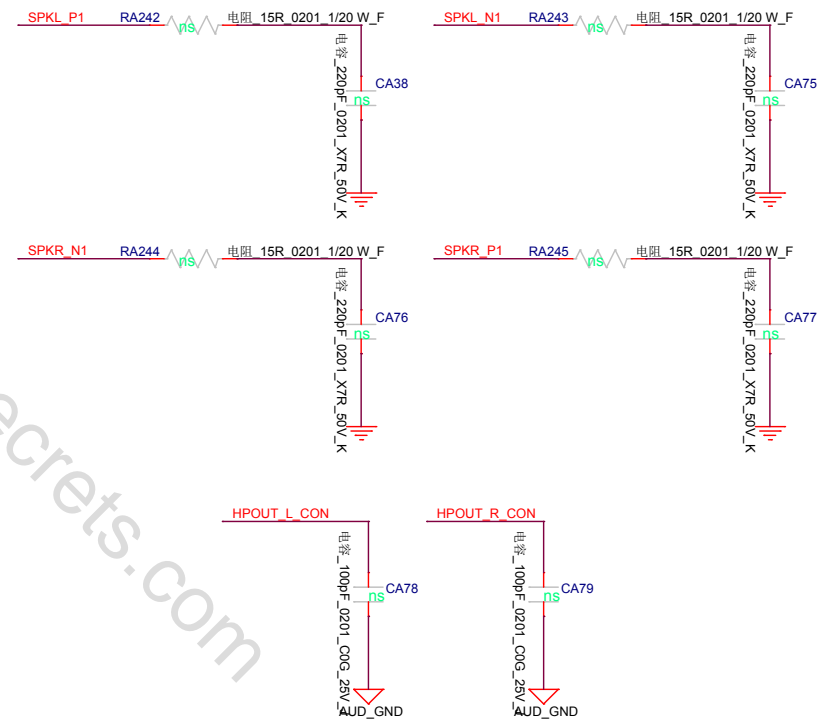
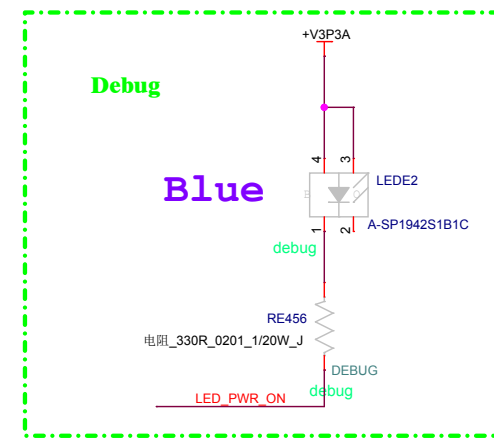
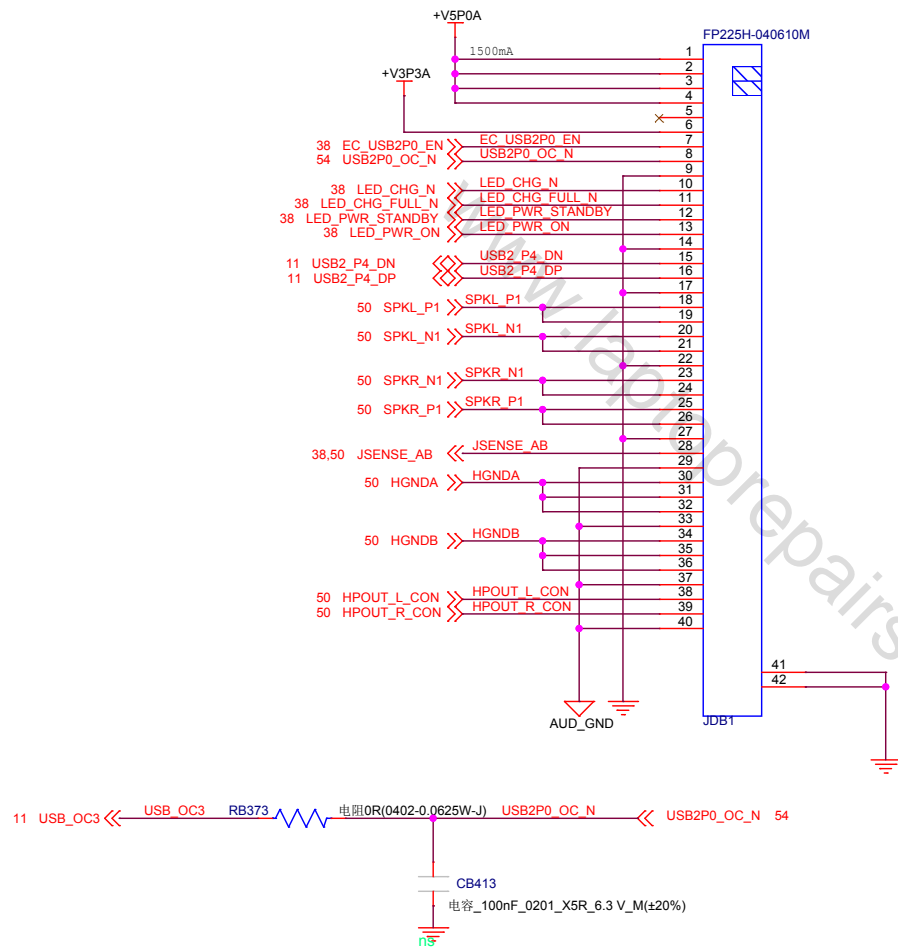
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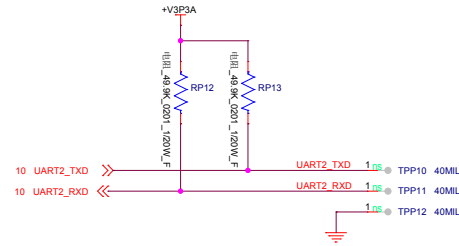
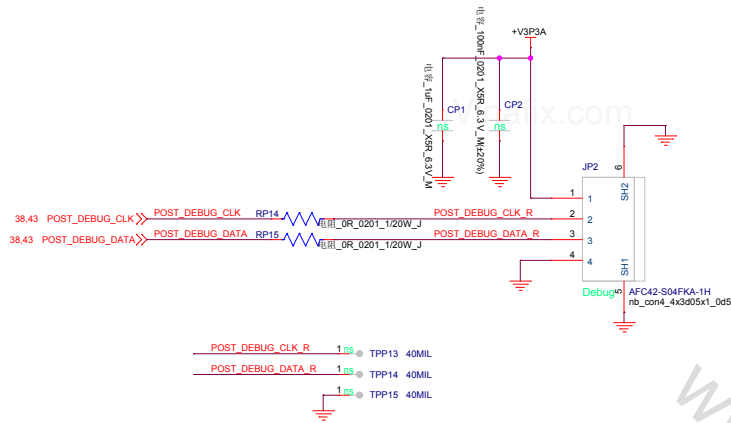


HALL



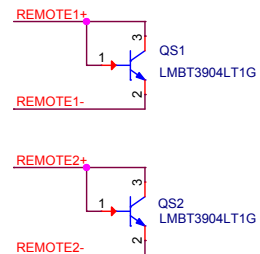
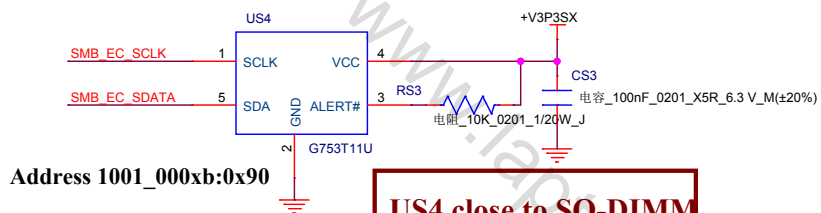
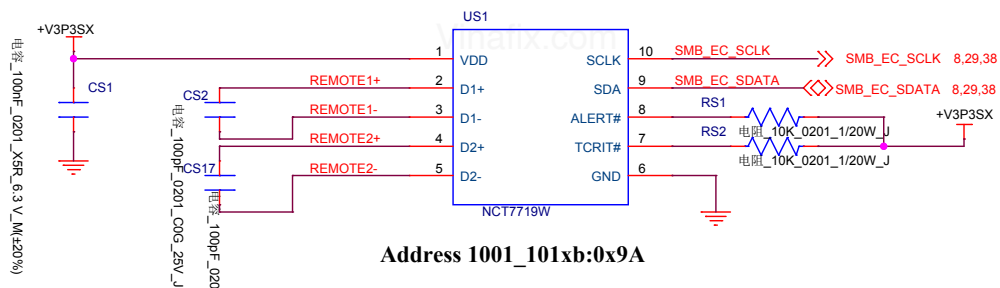
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| Huaqin Telecom Technology Com.,Ltd. |                      |           |  |
| Page name: G-SENSOR/FAN/LED/Hall    |                      |           |  |
| Size: A4                            | Project Name: NB8511 | REV: V1.0 |  |
| Date: Monday, July 15, 2019         | Sheet: 53            | of 72     |  |





REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"  
Connect guard traces to GND on either side of the  
DXP-DXN traces

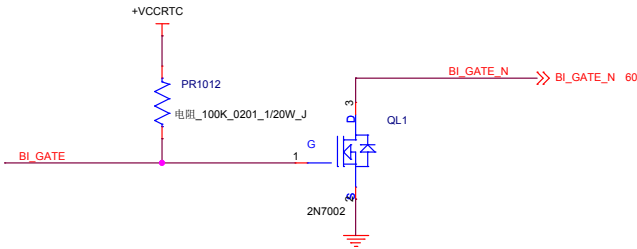
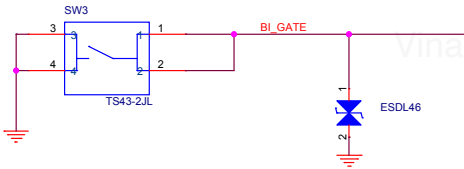
Close to charger



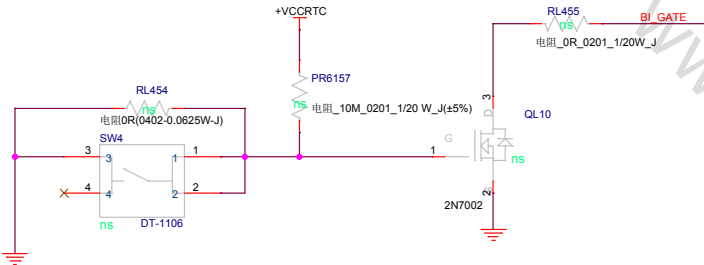
Between CPU and GPU



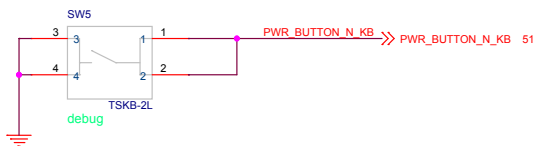
Reset BUTTON



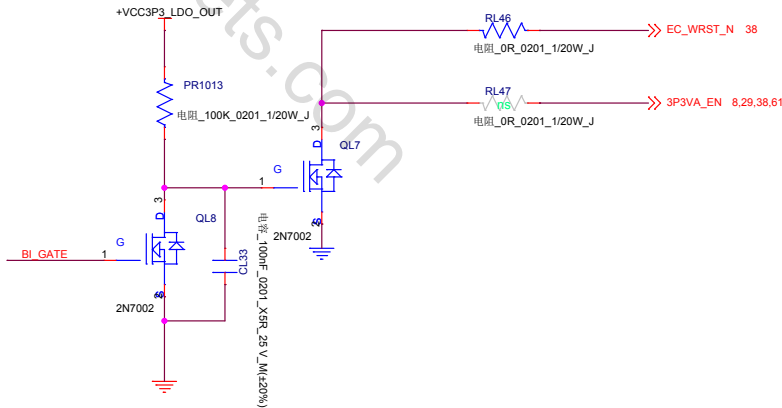
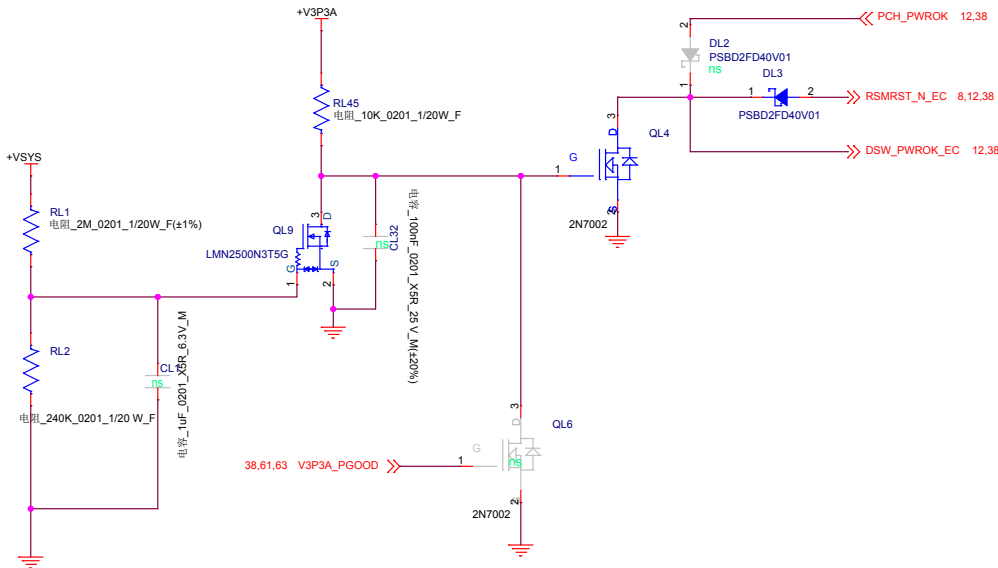
Open door BUTTON



Debug BUTTON



Abnormal PD logic



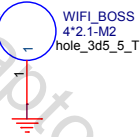
CPU螺母元件 \*4



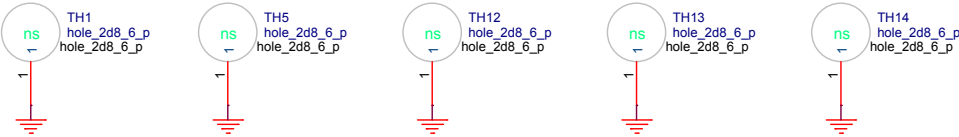
GPU螺母元件 \*2



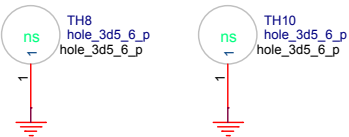
WIFI螺母元件 \*1



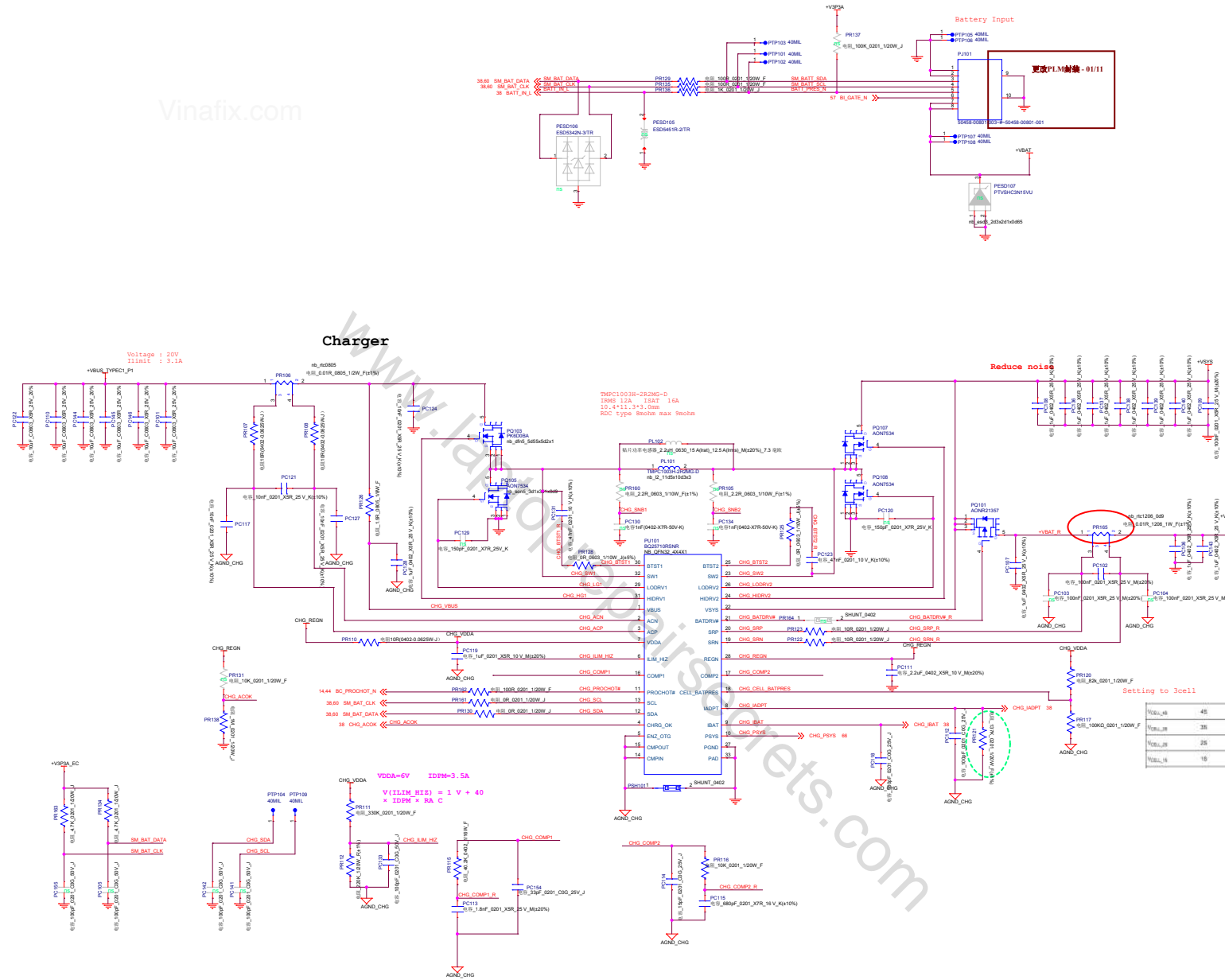
HOLE \*5



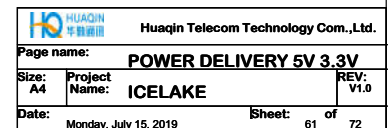
HOLE \*2

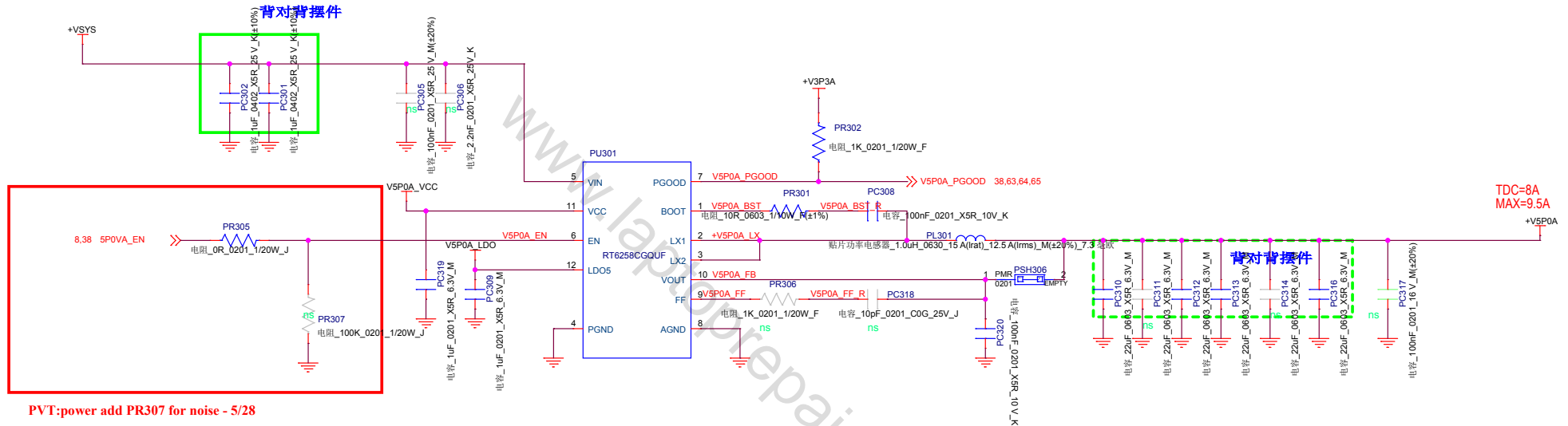


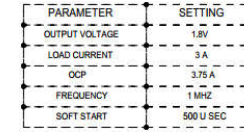


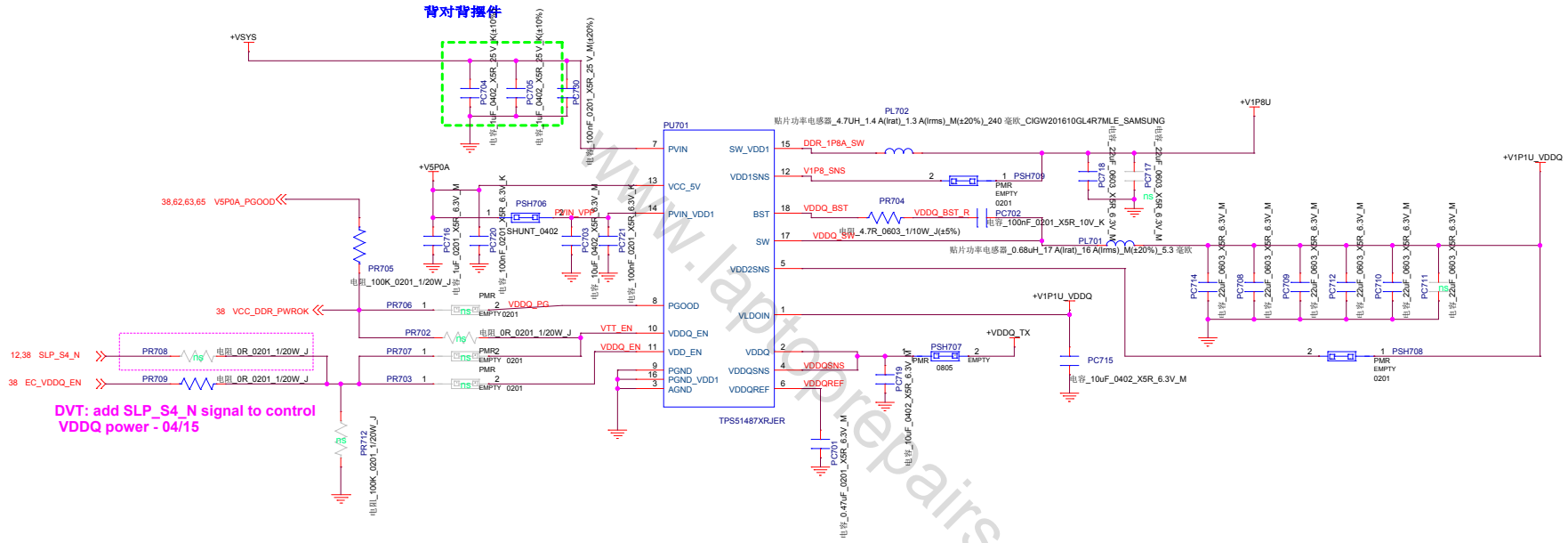


Voltage : battery cell TSD  
I<sub>max</sub> : 0.0000A  
I<sub>min</sub> : 6.45A  
I<sub>OC</sub> : TSD  
OCF : TSD



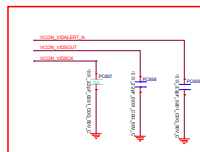
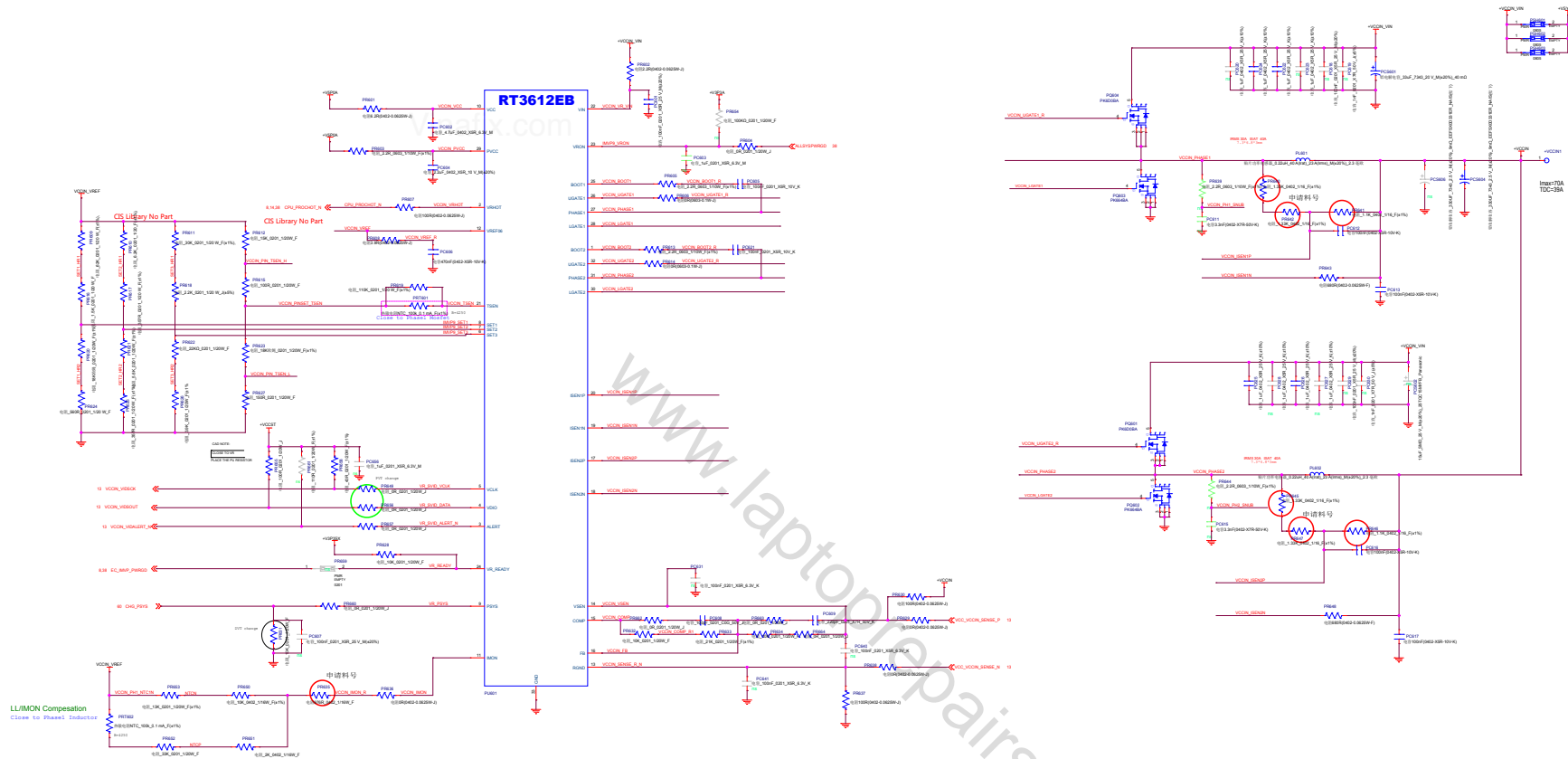


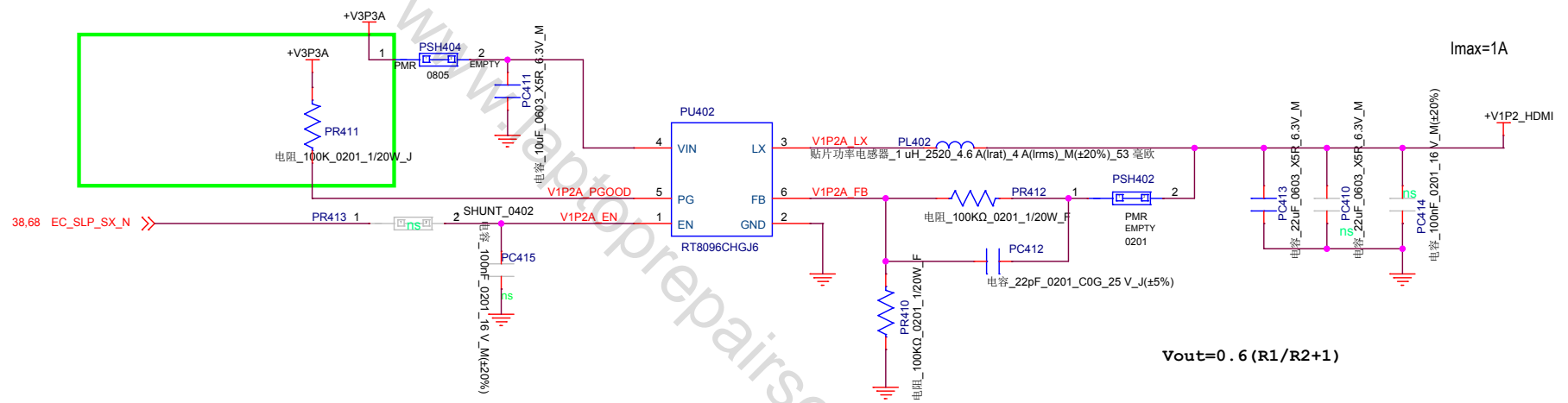


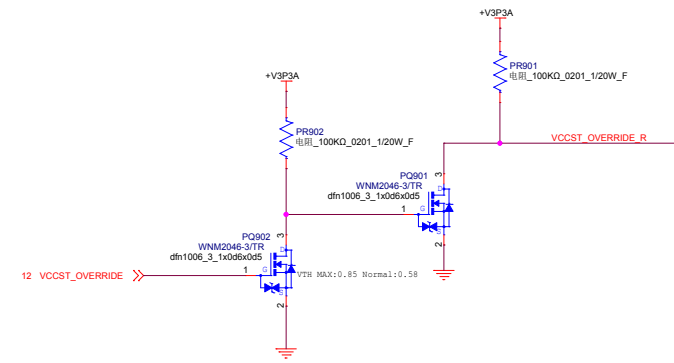
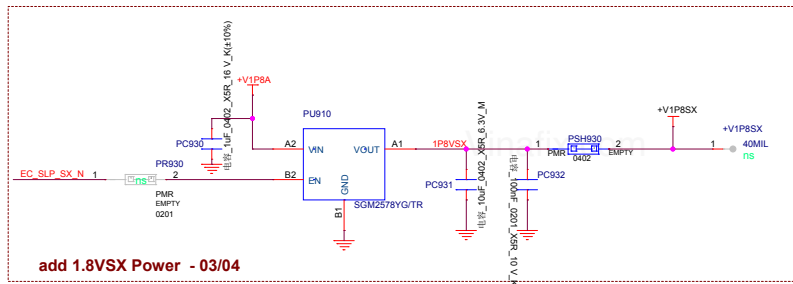




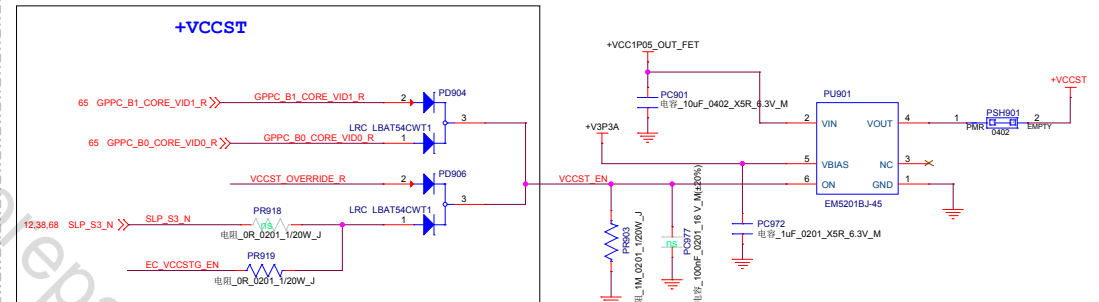
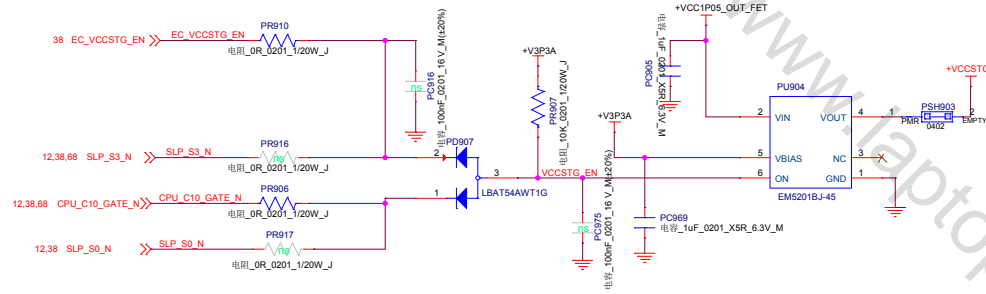




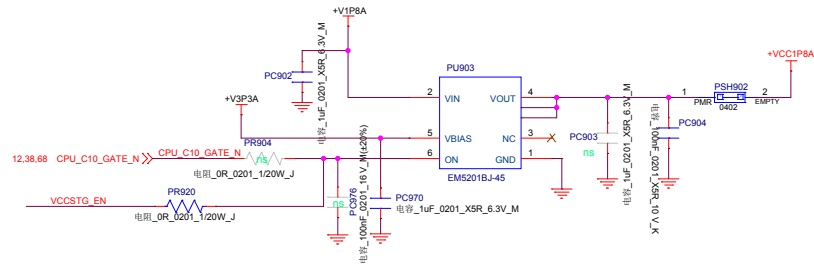




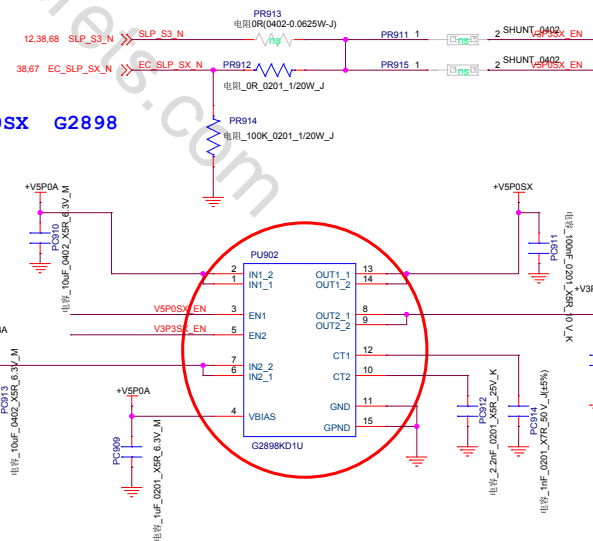
## +VCCSTG\_IO



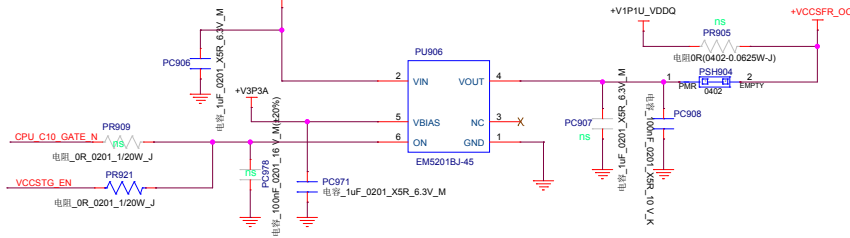
## +VCC1P8A



## +V3P3SX, +V5P0SX G2898



## +VCCSFR\_OC



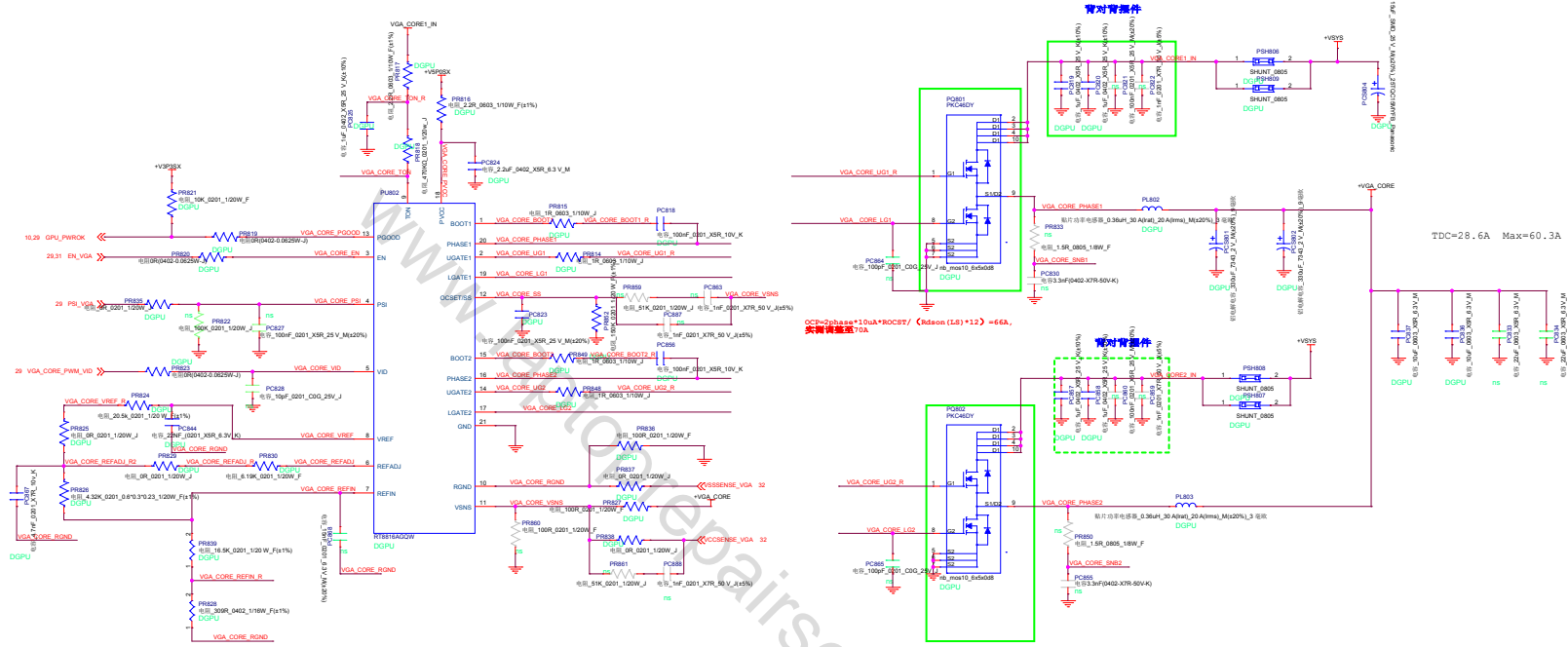
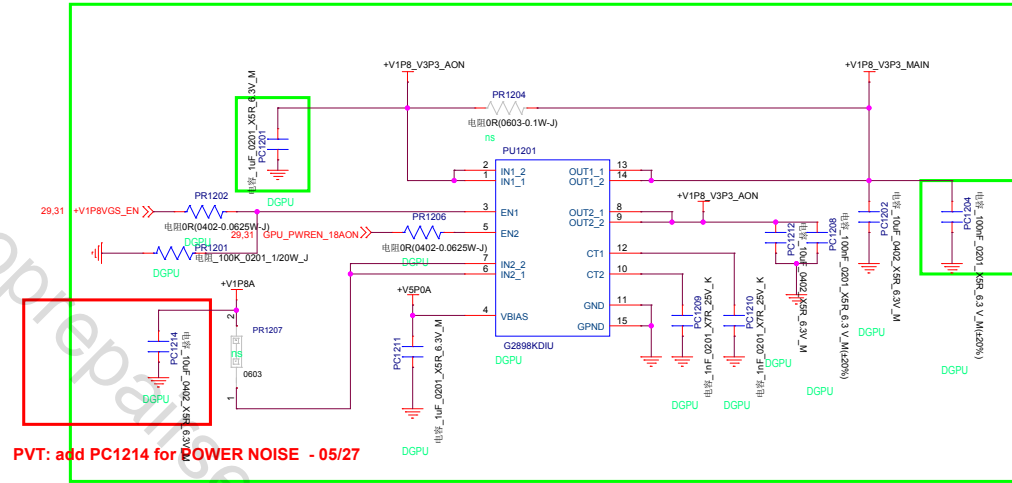
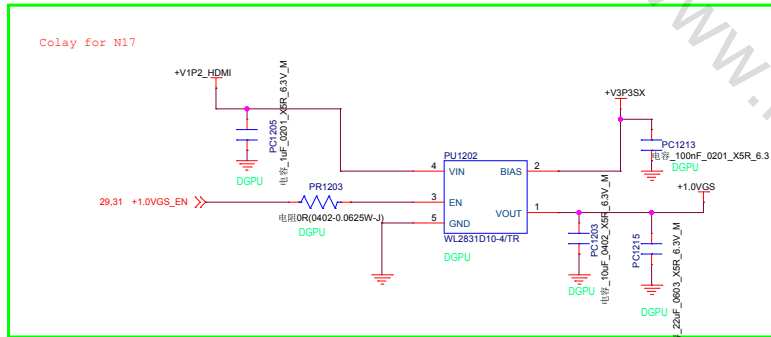


Table 7. Output EDP-Continuous


|                      | NVVD | GPU FBIO           | FB.Total <sup>5</sup> | 1.0V Total <sup>1</sup> | 1.8V Total <sup>2</sup> |
|----------------------|------|--------------------|-----------------------|-------------------------|-------------------------|
|                      | —    | 1.35V <sup>4</sup> | 1.35V <sup>4</sup>    | 1.0V <sup>4</sup>       | 1.8V <sup>4</sup>       |
| Product              | (A)  | (A)                | (A)                   | (A)                     | (A)                     |
| N17S-LG              | 15.4 | 2.5                | 5.0                   | 0.1                     | 0.2                     |
| N17S-G1              | 30.0 | 3.0                | 5.6                   | 0.1                     | 0.3                     |
| N17S-G0 <sup>6</sup> | 27.8 | 3.2                | 5.8                   | 0.2                     | 0.5                     |
| N17S-G2 <sup>6</sup> | 28.6 | 3.2                | 5.8                   | 0.2                     | 0.5                     |

Table 8. Output EDP-Peak

|                      | NVVD | GPU FBIO           | FB.TOTAL <sup>4</sup> | 1.0V Total <sup>1</sup> |
|----------------------|------|--------------------|-----------------------|-------------------------|
|                      | —    | 1.35V <sup>3</sup> | 1.35V <sup>3</sup>    | 1.0V <sup>3</sup>       |
| Product              | (A)  | (A)                | (A)                   | (A)                     |
| N17S-LG              | 48.3 | 2.8                | 5.8                   | 0.2                     |
| N17S-G1              | 60.1 | 3.4                | 6.9                   | 0.2                     |
| N17S-G0 <sup>6</sup> | 42.0 | 3.9                | 7.4                   | 0.3                     |
| N17S-G2 <sup>6</sup> | 60.3 | 3.9                | 7.4                   | 0.3                     |




PR1150:0Ω-10kΩ  
PC1150:100pF-1nF 11/5

|   |                                       |  |  |
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| <b>Page name:</b> <b>POWER DELIVERY 1.35VGS</b>                                       |                                       |  |  |
| <b>Size:</b><br><b>A4</b>   | <b>Project Name:</b><br><b>NB8511</b> | <b>REV:</b><br><b>V1.0</b>                 |  |
| <b>Date:</b><br><b>Monday, July 15, 2019</b>  | <b>Sheet:</b><br><b>71</b>            | <b>of</b><br><b>72</b>                     |  |

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| Page name: <b>BLANK</b>   |                                |                                     |              |
| Size:<br>A4   | Project<br>Name: <b>NB8511</b> |                                     | REV:<br>V1.0 |
| Date: <b>Monday, July 15, 2019</b>  |                                | Sheet: <b>72</b>                    | of <b>72</b> |